LC Detector R&D: Report from Liaisons

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Maxim Titov (CEA Saclay)

Plenary Talk, Belgrade, Serbia, October 6, 2014

LC Detector Challenges: The Higgs is an Important Driving Factor

June 2013: Detailed Baseline Design (DBD) for Detectors
http://www.linearcollider.org/ILC/Publications/Technical-Design-Report

- ❖ Key detector R&D technologies have been demonstrated with prototypes in test beams;
- ❖ Physics performance has been studied in full simulations

- ❖ The ILC DBD is NOT a Detector TDR
  → missing detailed engineering; ILD/SiD optimizat.
- ❖ Not all R&D has been completed
  → R&D remains an active field

❖ VERTEX: flavour tag, IP resolution (H → bb, cc ττ)
~1/5 $r_{beampipe}$,1/30 pixel size, ~1/10 resolution (ILC vs LHC)

$$\sigma_{IP} = 5 \oplus \frac{10}{p \sin^{3/2}\theta} (\mu m)$$

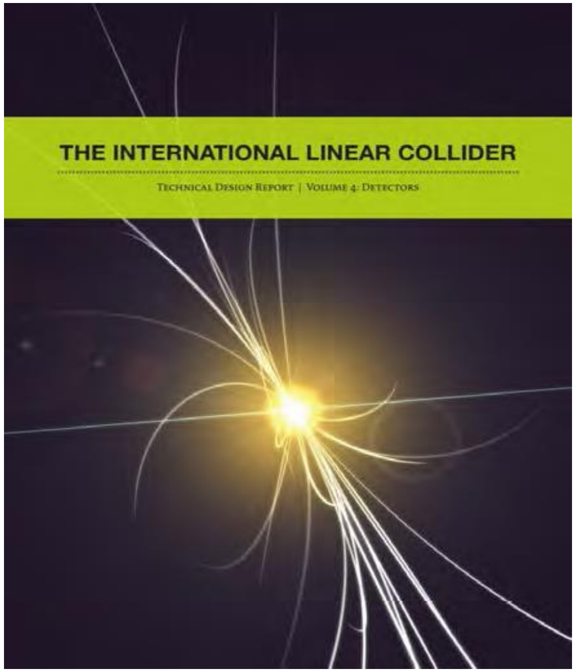
❖ TRACKING: recoil mass to Higgs (e+e- → ZH → llX)
~1/6 material, ~1/10 resolution (ILC vs LHC); B = 3.5 – 5T

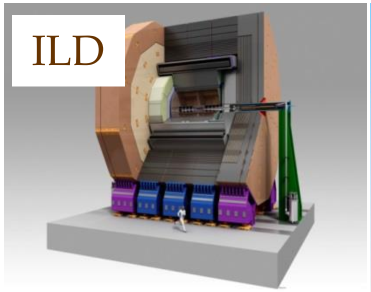
$$\sigma(1/p) = 2 \times 10^{-5} (\mathrm{GeV}^{-1})$$

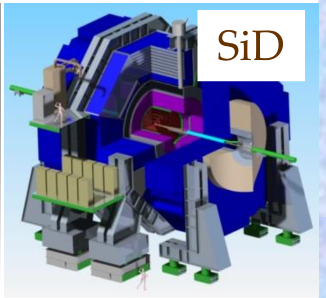
❖ CALORIMETRY: particle flow, di-jet mass resolution
1000x granularity, ~1/2 resolution (ILC vs LHC);
detector coverage down to very low angle

$$\sigma_E / E = 0.3/\sqrt{E(\mathrm{GeV})}$$

"Push-pull Option" – 2 detectors:
similar concepts /
different realizations
(central tracking with Si or TPC)
Cost constrained design choices







RPC DHCAL

Scintillator ECAL

SPiDeR

Collaborations

FCAL

CLICPix

DEPFET

LCTPC

SOI

ChronoPixel

SDHCAL

TPAC

RPC Muon

GEM DHCAL

KPIX

Silicon ECAL (SiD)

VIP

Silicon ECAL (ILD)

Dual Readout

CMOS MAPS

DEPFET Active Pixel Detector

CALICE Calorimeter for ILC

FPCCD

FCAL Collaboration High precision design

Scintillator HCAL

Many forms of Detector R&D relevant to LC:

- Large collaborations such as CALICE,LCTPC,FCAL
- Collection of many efforts such as the vertex R&Ds
- Individual group R&D activities
- Efforts currently not directly included in the concept groups (ILD, SiD, CLIC), which may become important for LC in future

NB: incomplete list. For illustration purposes only.

ECFA Detector R&D Panel – A European Committee to Review R&D Efforts for Future Projects

Review of ILC R&D Efforts (http://ecfa-dp.desy.de):

- May 2-3, 2012: Different R&D
  https://indico.desy.de/conferenceDisplay.py?confId=5800
- Nov. 5, 2012: CALICE R&D
  https://indico.desy.de/conferenceDisplay.py?confId=6830
- Jun. 10, 2013: FCAL R&D
  https://indico.desy.de/conferenceDisplay.py?confId=7893
- Nov. 4-5, 2013: LCTPC R&D
  http://indico.desy.de/conferenceDisplay.py?confId=8573
- Jun. 11-12, 2014: Vertex Detector R&D
  https://indico.desy.de/conferenceDisplay.py?confId=10026

ECFA Detector R&D Panel
LCTPC
Review Report

LCTPC: ~ 70 pages

LCTPC collaboration

LC-DET-2014-001

November 3, 2013

arXiv: 1212.5127

Calorimetry for Lepton Collider Experiments – CALICE results and activities*

The CALICE Collaboration

CALICE: ~ 70 pages

Abstract

The CALICE collaboration conducts calorimeter R&D for highly granular calorimeters, mainly for their application in detectors for a future lepton collider at the TeV scale. The activities ranges from generic R&D with small devices up to extensive beam tests with prototypes comprising up to several 100000 calorimeter cells. CALICE has validated the performance of particle flow algorithms with test beam data and delivers the proof of principle that highly granular calorimeters can be built, operated and understood. The successes achieved in the past years allows the step from prototypes to calorimeter systems for particle physics detectors to be addressed.

Status Report

FCAL Collaboration

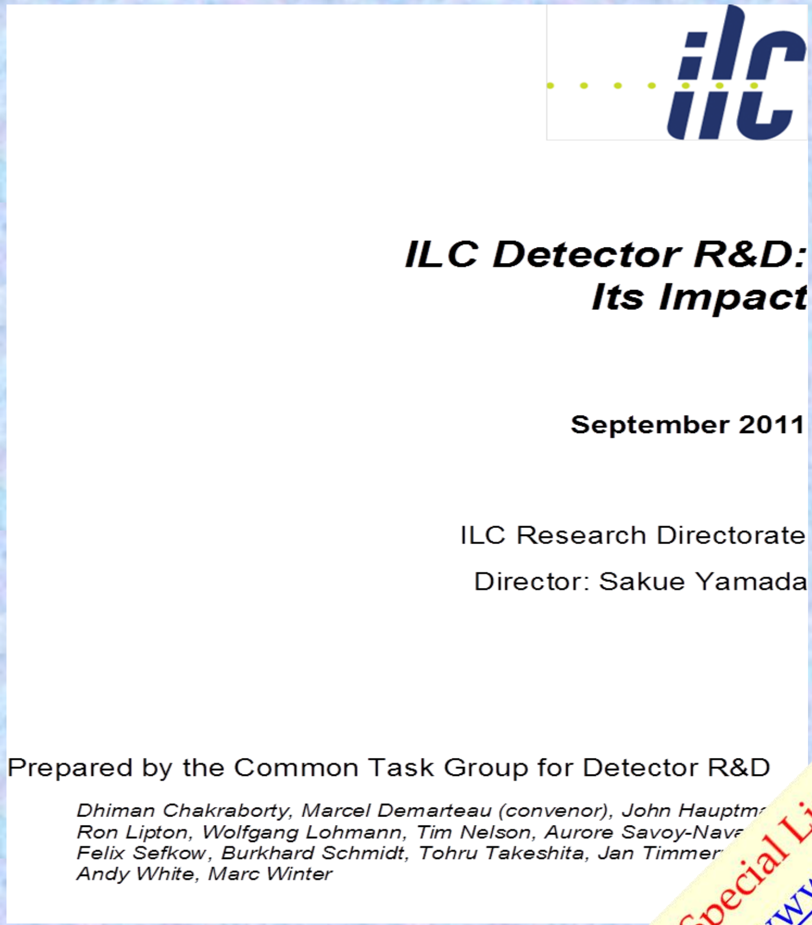
June 2013

FCAL: ~ 70 pages

Abstract

Two special calorimeters are foreseen for the instrumentation of the very forward region of an ILC or CLIC detector; a luminometer (LumiCal) designed to measure the rate of low angle Bhabha scattering events with a precision better than 10^{-3} at the ILC and 10^{-2} at CLIC, and a low polar-angle calorimeter (BeamCal). The latter will be hit by a large amount of beamstrahlung remnants. The intensity and the spatial shape of these depositions will provide a fast luminosity estimate, as well as determination of beam parameters. The sensors of this calorimeter must be radiation-hard. Both devices will improve the e.m. hermeticity of the detector in the search for new particles. Finely segmented and very compact electromagnetic calorimeters will match these requirements. Due to the high occupancy, fast front-end electronics will be needed.
Monte Carlo studies were performed to investigate the impact of beam-beam interactions and physics background processes on the luminosity measurement, and of beamstrahlung on the performance of BeamCal, as well as to optimise the design of both calorimeters.
Dedicated sensors, front-end and ADC ASICs have been designed for the ILC and prototypes are available. Prototypes of sensor planes fully assembled with readout electronics have been studied in electron beams.

ILC Detector R&D: Spin-Offs is a Key Word to Survive


ILC Detector R&D:
Its Impact

September 2011

ILC Research Directorate

Director: Sakue Yamada

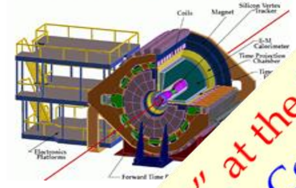
Prepared by the Common Task Group for Detector R&D

Dhiman Chakraborty, Marcel Demarteau (convenor), John Hauptm…
Ron Lipton, Wolfgang Lohmann, Tim Nelson, Aurore Savoy-Nava…
Felix Sefkow, Burkhard Schmidt, Tohru Takeshita, Jan Timmer…
Andy White, Marc Winter

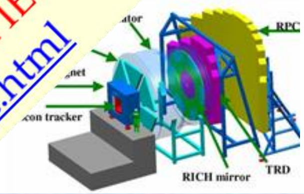
Major Impact in HEP Domain Beyond ILC:

CMOS-MAPS Initial Objective: ILC (with staged performance)
→ applied to hadron experiments with intermediate requirements (STAR, ALICE, C…

STAR 2012
Solenoidal Tracker @ RHIC (~ 1600 cm2)

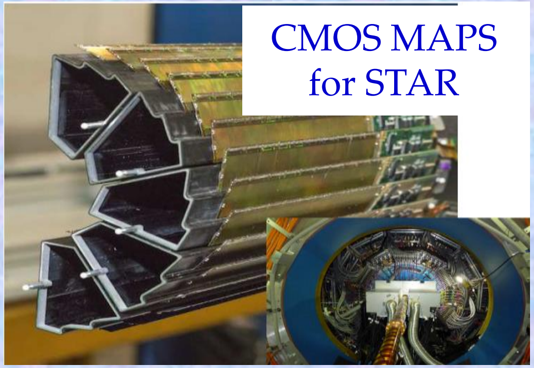


C… …aryonic … …00 cm2)



ALICE 2018
A Large Ion Colliderr (Inner Tracker System):

DEPFET for Belle II



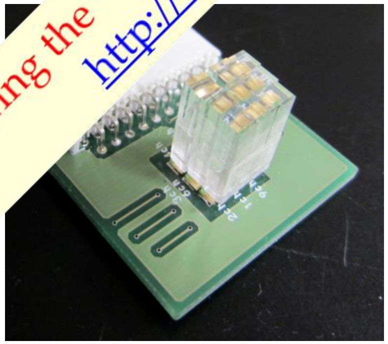
CMOS MAPS for STAR

Also during the “Special Linear Collider Event” at the 2012 IEEE NSS/MIC:
http://www.desy.de/~nss2012/2012LCevent.html

… Outside High Energy Physics:

Prototype for PET Applications

3x3 array of … crystals … SiPMs (30… time resolution):



TRECAM (Tumor Resection CAMera): miniaturized gamma-camera for breast cancer surgery

49 x 49 mm² field of view
$LaBr_3$:Ce crystal optically coupled to a multi-anode photomultiplier tube

Detector R&D Liaison Report

LCC PHYSICS AND DETECTORS EXECUTIVE BOARD:
→LC DETECTOR R&D LIAISONS: Maxim Titov (Liaison), Jan Strube (Deputy Liaison)

CHARGE:

- The detector R&D liaison ensures productive communication between the LCC Physics and Detectors Executive Board and detector R&D groups. The liaison is a member of the Executive Board and communicates relevant information from the Executive Board to detector R&D groups and vice versa.

- The liaison is in contact with all detector R&D groups relevant to linear colliders to keep track of the overall detector R&D efforts conducted or planned for linear colliders and to periodically compile summaries of the efforts.

Detector R&D Liaison Report: get an overview over the LC Detector R&D Efforts

- Update of the R&D developments since ILC DBD and CLIC CDR
- "Publicize" the technology. Summarize contributions of individual R&D efforts.
  → Make areas of overlap obvious without pointing out (not an attempt to control diff. R&Ds)
- Provide a "showcase" for the technology. Manpower and financial resources are explicitly not mentioned in the report.
- Provide an entry point for new groups →help them to learn the current landscape of the LC R&D efforts and the areas where they can contribute

Detector R&D Liaison Report

Individual ILC / CLIC R&D Groups were asked to provide a few pages summary (5 questions):

- Introduction. Brief overview of the technology (past R&D efforts with references)
- Recent developments since ILC DBD / CLIC CDR (to avoid receiving historical data);
- Engineering challenges (for putting the technology into a real-world LC detector)
- Future Detector R&D activities in the years to come.
  List of collaborating institutes (contributing to the given R&D technology)
- Application of the R&D outside of ILC (with references, if technology is already used)

R&D Technology	Participating Institutes	Description / Concept	Achieved Results / Milestones :	Future Activities :
ILC DBD or CLIC CDR Concept:		… and were asked to summarize major activities in the table:		

- ❖ Concentrate on the R&D activities for the ILD/ SiD Concepts
- ❖ Discuss synergy between ILC and CLIC developments (whenever possible)
- ❖ Group individual R&Ds based on vertexing, tracking, calorimetry, …

Detector R&D Liaison Report: Overview

- ~ 30 individuals R&D groups contacted → ensure maximum coverage of technologies (~20)
  → see details in the Detector R&D Liaison Report at LCWS in Chicago (May, 2014)

- List of responses was rather variable → from pointers to past publications to 100+ page documents; from text in the mail to bullet points and to 18+ dedicated pages
  → Contributions came in many format (LaTeX, Word, PDF, emailed text, …) with varying quality of references

- Detector R&D Liaison Report is being written in LaTeX.
  → Currently 60+ pages + 7 pages references. Goal was ~ 70 pages.

- Software in the Detector R&D Report → suggested at the SiD meeting (Sept. 2014)

  → This can be a huge benefit. We contacted Norman Graf, Frank Gaede, Akiya Miyamoto
  → Norman agreed to coordinate with the other members of the Software and Computing Group to compile this contribution (DD4HEP, SLIC, LCFIPlus, PandoraPFA, …)

Similar 5 questions to be addressed:

- Introduction/Overview: Recent Highlights (in DBD / CDR or later); examples of use, for reco: precision achieved
- Engineering challenges: performance limitations in terms of memory, CPU scaling performance with more complex events, file size, …
- Status and Plans; List of collaborating institutes
- Examples of Applications outside of LC

Detector R&D Liaison Report: Summary Tables

The current layout makes it still difficult to get a quick overview.

We are working on a summary tables listing collaborating institutions, milestones, future plans.
This will become the main part of an executive summary for each section (not each technology).

R&D Technology	Participating Institutes	Description/ Concept	Milestones	Future Activities
CMOS MAPS	IPHC Strasbourg	The CMOS pixel sensor uses as a sensitive volume the 10-20 μm thin high-resistivity epitaxial Si-layer deposited on low resistivity substrate of commercial CMOS processed chips. The generated charge is kept in a thin epi-layer atop the low resistivity silicon bulk by potential wells that develop at the boundary and reaches an n-well collection diode by thermal diffusion.		
DEPFET	IFCA IFIC Valencia Barcelona Univerity Bonn University	The DEPFET technology implements a single active element within the active pixel by integrating a p-MOS transistor in each pixel on the fully depleted, detector-grade bulk silicon. Additional n-implants near the transistor act as a trap for charge carriers created in the substrate (internal gate), so that they are collected beneath the transistor gate.	Full-scale 75 μm thin Belle II ladder in beam test at DESY 2014	Development of die-attach technology Full-scale test of all ASICs on ladder Integration of read-out and steering ASICs on pixel sensor using flip-chip technique and microscopic solder ball bump-bonding Production of Belle II vertex detector modules Tests of the last version of the DHP chips Engineering design for all-silicon module with petal geometry required for ILC Detailed characterization of device response Design of ancillary ASICs, taking full responsibility for future design cycles of the FE read-out chip, called Drain Current Digitizer
FPCCD	KEK Tohoku University Shinshu University JAXA, Japan Aerospace Exploration Agency	Fine Pixel CCD sensors have pixel sizes of 5 μm and a fully depleted epitaxial layer with a thickness of 15 μm.	Fabrication of real size (12.3 mm x 62.4 mm) sensors with 50 μm total thickness Neutron irradiation of a small (6 mm x 6 mm) FPCCD sensor Construction of a prototype cooling system and demonstration of cooling between -40°C and +15°C	Characterization of FPCCD sensors including beam tests and radiation damage studies Development of FPCCD sensors with a pixel size of 5 μm Construction of prototype ladders for the inner layers of a vertex detector Development of readout electronics downstream of ASICs Development of larger FPCCD sensors and prototype Development of readout electronics with a small footprint Construction of a real size engineering prototype and cooling test
ChronoPix	University of Oregon Yale University Sarnoff Corporation	ChronoPix is a monolithic CMOS pixelated sensor with the ability to record up to two time stamps per pixel	Device tests of Prototype 2 inform the design of Prototype 3 to be submitted to foundry by the end of April 2014	Improve S/N to at least 20 Further reduce pixel size from 25 μm to eventually 15 μm. Requires feature size less than 65 nm Reduce inter-pixel and digital-to-analog circuit cross talk and parasitic feedback
3D Pixels	Brown University Cornell University Fermilab Northern Illinois University SLAC University of Illinois Chicago	3D technology allows very fine pitch (4 μm) integration of sensors with multiple layers of electronics, allows interconnection oto both the top and bottom of devices, and provides techniques for low mass, thinned devices.	Completed multi-year effort to demonstrate commercial 3D technology, consisting of 0.13 μm CMOS interconnected with Direct Oxide bonding technology and access using Received readout wafers with thickness of 25 μm, processed with TSV and DBI to connect to 3D electronics Currently working on active edge demonstrator devices	Complete the 3D active edge project Apply concepts to x-ray imaging devices Re-start ILC developments pending renewed funding
SOI	KEK	In the Silicon-On-Insulator (SOI) technology the sensing and processing functionalities are separated in different		Sep 2014: Complete architecture study for the ILC pixel detector Mar 2015: Design and fabrication of first test chip for the Dec 2015: Beam test of the chip
CLICPix	CERN Spanish Network for Future Linear Colliders University of Liverpool Institute of Space Science, Bucharest University of Bristol	A detector concept is based on hybrid planar pixel-detector technology. It comprises fast, low-power and small-pitch readout ASICs implemented in 65 nm CMOS technology. The target thickness for both the sensor and readout layers is only 50 mm each. Slim-edge sensor designs are under study and TSV technology is foreseen for vertical interconnection.		Development of hybrid pixel readout ASIC with 25 μm pitch, analog readout, time stamping and power pulsing functionality, implemented in 65 nm CMOS technology Development of ultra-thin (50 μm) planar pixel sensors, as well as active sensors with capacitive coupling Low-mass fine-pitch interconnects between sensor and Through-silicon-via technology for powering, configuration and readout of the ASIC Low-mass powering infrastructure, including power-pulsing with local energy storage Low-mass carbon fiber supports Detector cooling based on forced air flow Concepts for mechanical integration and detector assembly Detector layout optimization studies

Detector R&D Liaison Report: Current Status

- We need some additional help if we are to meet our goal of ~70 pages:

→ If **<u>your chapter is not shown in green</u>** (see later in "Summary of Contributions") → <u>we contact you or please talk to us.</u>

Contents

Preliminary

... Already Some References to the Detector R&D Liaison Report

2014 ICHEP Conference: http://ichep2014.es

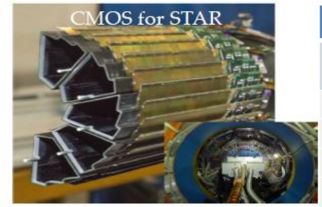
Detector R&D

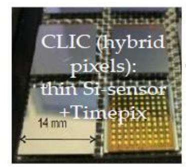
Phil Allport
(Liverpool University)

- Tracking Detectors
  - Silicon Vertex Detectors
  - Silicon Tracking Detectors
  - Gaseous Detectors (Trackers and Muon Spectrometers)
- Calorimeters
  - ILC/CLIC R&D
  - HL-LHC R&D
- Fast Timing and Particle Identification Techniques
- Read-out and Triggering
- Neutrino Detectors
  - Technologies
  - Instrumenting Very Large Volumes
- Conclusions

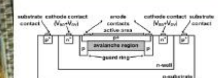
Silicon Vertex Detector R&D for ILC/CLIC

Report from the ILC R&D Liaison
(AWLC, Fermilab, May 12 - 16, 2014)



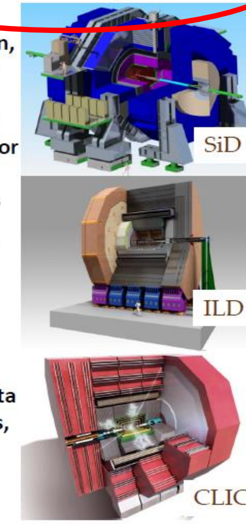


Technologies
ILC Pixel Vertex R&D:
CMOS MAPS
DEPFET
FPCCD
3D-pixel and integration
Chronopixel
SoI
CLIC Pixel Vertex R&D:
Hybrid Sensor +ASIC, HV-CMOS + ASIC
GAPD



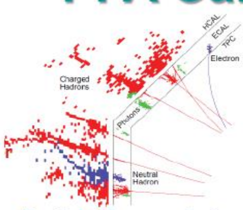
Challenges of ≤ 5µm precision, extremely low material and time-stamping given accelerator bunch train time structures ILC-500 (1312 at 554ns every 200ms) CLIC (312 at 0.5ns every 20ms)

→ Different on-detector data storage options, integration technologies and powering schemes



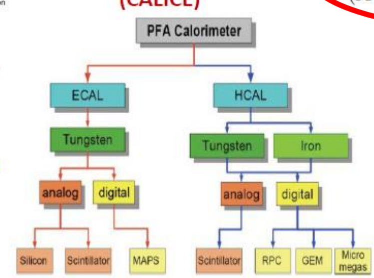
PFA Calorimeter R&D for ILC/CLIC

Report from the ILC R&D Liaison
(AWLC, Fermilab, May 12 - 16, 2014)



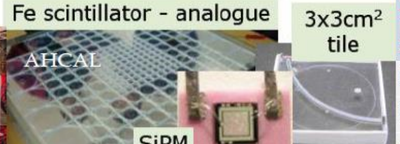
Particle flow analysis: need to associate energy deposits with charged particles → drives granularity requirements

Particle Flow Calorimetry (CALICE)



Fe scintillator - analogue

3x3cm² tile



$\sigma/E \approx 45\%/\sqrt{E} \oplus 1.7 \oplus 0.18/E$

Si-ECAL: $\sigma/E \approx 17\%/\sqrt{E} \oplus 1.7$

Technology
ILC ECAL R&Ds:
Silicon ECAL
MAPS ECAL
Sci ECAL
ILC HCAL (AHCAL) R&Ds:
Sci AHCAL
ILC HCAL ((s)DHCAL) R&Ds:
RPC DHCAL
RPC sDHCAL
GEM DHCAL
MM sDHCAL

ILC Forward Calorimeter R&Ds:
LumiCal / BeamCal
Dual-readout calorimetry
Technology
CLIC HCAL R&Ds:
Sci AHCAL
RPC DHCAL
CLIC FCAL R&Ds:
FCAL hardware

Gaseous Tracking Detector R&D

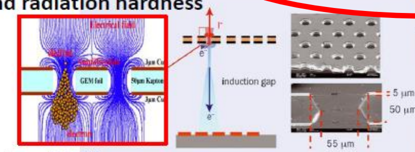
Report from the ILC R&D Liaison
(AWLC, Fermilab, May 12 - 16, 2014)

Main R&D activities for ATLAS and CMS are for new muon chambers in the forward directions.

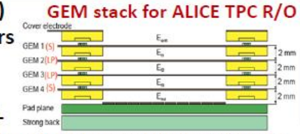
- Increased rate capabilities and radiation hardness
- Improved resolution (online trigger and offline analyses)
- Improved timing precision (background rejection)

Technologies

- Gas Electron Multiplier detectors (LHCb now, ALICE TPC - CMS forward chambers)
- Micro-pattern gas and Thin Gap Chambers (TGCs) (ATLAS forward chambers)
- Resistive Plate Chambers (RPCs) - low resistivity glass for rate capability - multi-gap precision timing (CMS forward chambers)

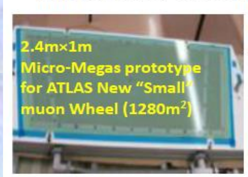


GEM stack for ALICE TPC R/O



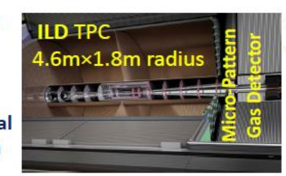
4 layer stack to minimise Ion backflow given continuous readout at 50kHz

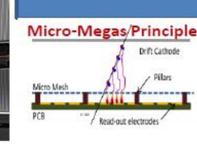
ILC Technologies
GEM- based readout:
Laser-etched GEM
Wet-etched GEMs
Micromegas-based readout:
Resistive MM with dispersive anode
GEM or Micromegas + Timepix pixel readout:
GEM + pixel
InGrid



CERN RD51 common to GEM and Micro-Megas (does not include RPC R&D)

Developing commercial large-scale production capabilites





ILC Detector Challenges: R&D Collaborations and Group Efforts

Individual R&D Efforts
(e.g. vertex detectors):

MAPS
CMOS

DEPFET Active Pixel Detector

FPCCD

Chronopixel

SOI

3D

"Horizontal R&D"
Collaborations:

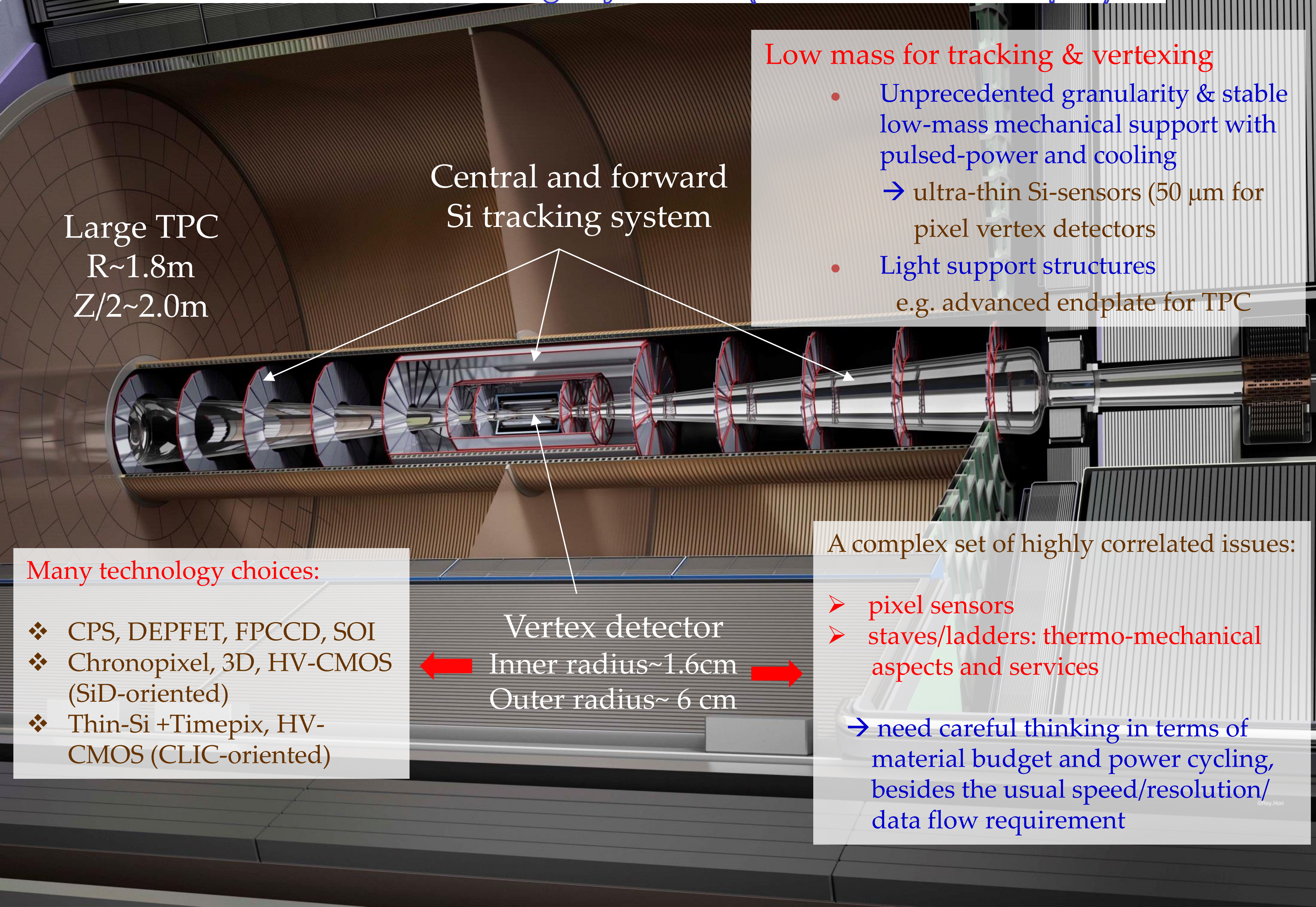
LC TPC
Time Projection Chamber for Linear Collider

FCAL Collaboration, High precision design
Forward calorimeters for Linear Collider

CALICE, Calorimeter for ILC
Highly granular calorimeters for Linear Collider

- A lot of R&Ds is being carried out both within the ILD/SiD and through the "horizontal R&D collaborations"
- In the following, selection of the recent R&D results is presented → not possible to make a comprehensive review → apologies if your R&D efforts are not shown this time

Vertex and Tracking Systems (ILD as an Example)



Low mass for tracking & vertexing

- Unprecedented granularity & stable low-mass mechanical support with pulsed-power and cooling
  → ultra-thin Si-sensors (50 μm for pixel vertex detectors
- Light support structures
  e.g. advanced endplate for TPC

Many technology choices:

- CPS, DEPFET, FPCCD, SOI
- Chronopixel, 3D, HV-CMOS (SiD-oriented)
- Thin-Si +Timepix, HV-CMOS (CLIC-oriented)

A complex set of highly correlated issues:

- pixel sensors
- staves/ladders: thermo-mechanical aspects and services

→ need careful thinking in terms of material budget and power cycling, besides the usual speed/resolution/ data flow requirement

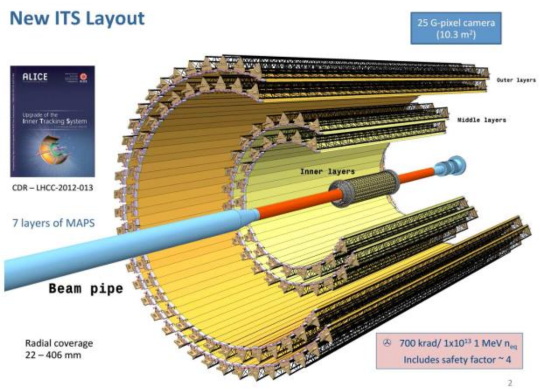
R&D on CMOS Pixel Sensors Adapted to an ILC Vertex Detector

M. Winter

STAR-PXL PHYSICS RUN OF SPRING '14

→ CPS validated for vertex detectors

→ sensor architectures developed in 0.35 μm CMOS process for ILD-VXD comply with DBD requirements



ALICE-ITS =NEW DRIVING APPLICATION OF CPS

based on a better suited (180 nm) CMOS process

(TDR approved by LHCC in March '14)

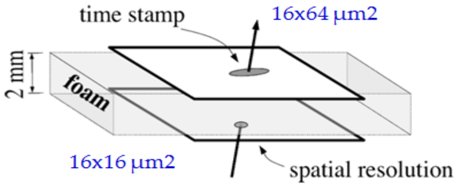
- 1^{st} real scale sensor prototype adapted to 10 m² fabricated
  - → 1st test results validate architecture in 180 nm technology
  - → 2-4 times faster read-out w.r.t. 0.35 μm technology, with up to 60 % power reduction

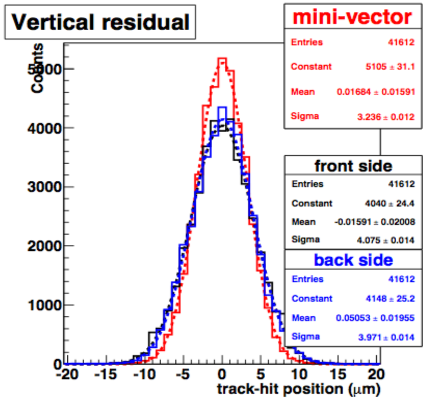
NEXT STEPS :

- Finalise ALICE-ITS sensor prototypes
- Derive CPS optimised for VXD:
  - → material bugdet, power-pulsing,
  - → target: bunch tagging

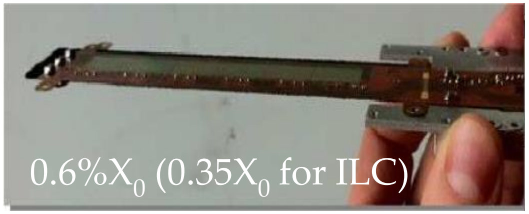
Layer	σ_{sp}	t_{int}
ILD-VXD/In (L1/L2)	$< 3 / 5\ \mu m$	$30\text{-}40 / 8 \mapsto < 1\ \mu s$
ILD-VXD/Out (L3-6)	$\sim 3.5 - 4\ \mu m$	$\lesssim 100\ \mu s$

CPS MAPS: Spatial Resolution and Time Stamping





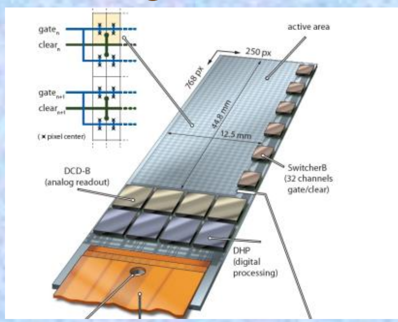
Ultrathin ladder - PLUME

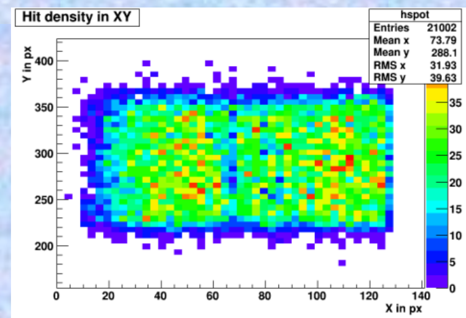


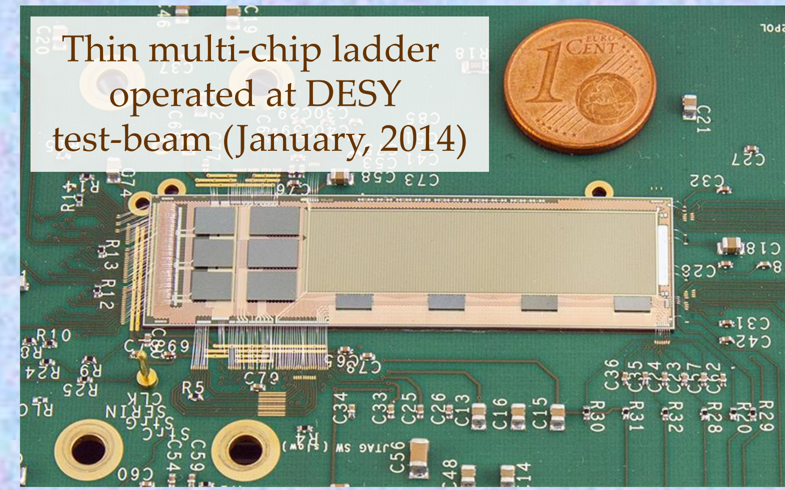
DEPFET R&D for ILC Vertex Detector

L. Andricek

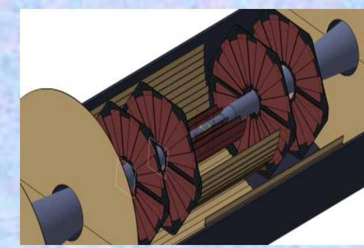
- ▷ DEPFET R&D for ILC vertex detector in the frame work of Belle II PXD construction
  - ↳ Pixel sensor design and auxiliary ASICs
  - ↳ Integration to low-mass modules



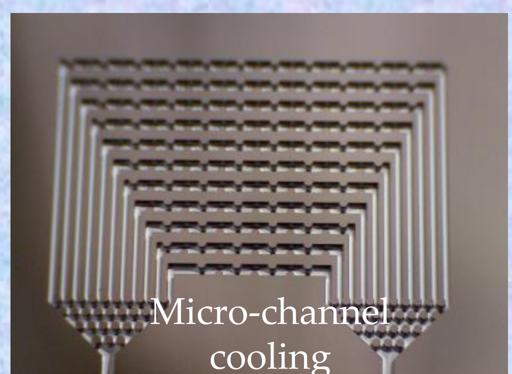


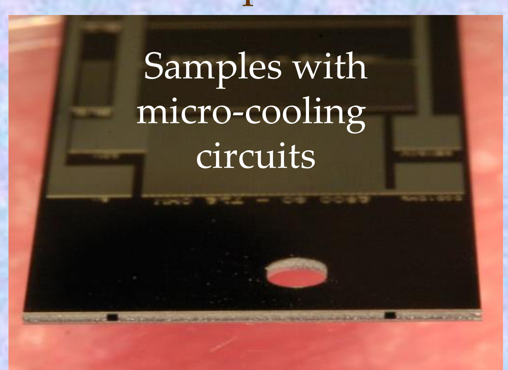


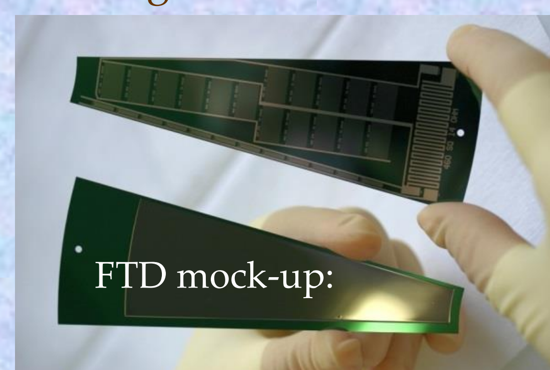
- ▷ Latest achievement
  - ↳ Large area thinned DEPFET sensor
  - ↳ full system test of Belle II vertex detector segment in the DESY beam



- ▷ New purely LC related activities
  - ↳ Silicon-integrated cooling channels
  - ↳ Extension of the all-silicon module concept to the vertex forward region







Chronopixel R&D and Status

J. Brau / N. Sinev

- ❖ Chronopixel design provides for single bunch-crossing time stamping (when signal exceeds threshold, time stamp provided by 14 bit bus)

- ➢ Prototype 1 (50x50 µm2 pixels, 180nm TSMC)

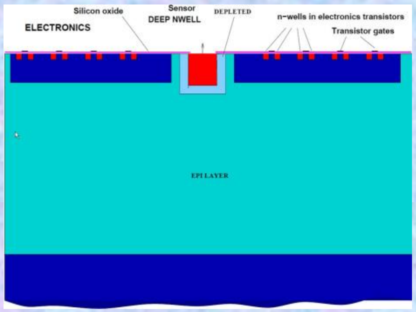
- ➢ Prototype 2 (25x25 µm2 pixels, 90nm TSMC)
  → Sensor capacitance larger than expected (because of design rules)

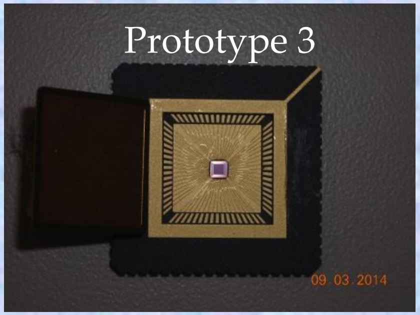
- ➢ Prototype 3 (25x25 µm2 pixels, 90nm TSMC
  → Six different sensor designs: Deep and shallow nwells and variations on design

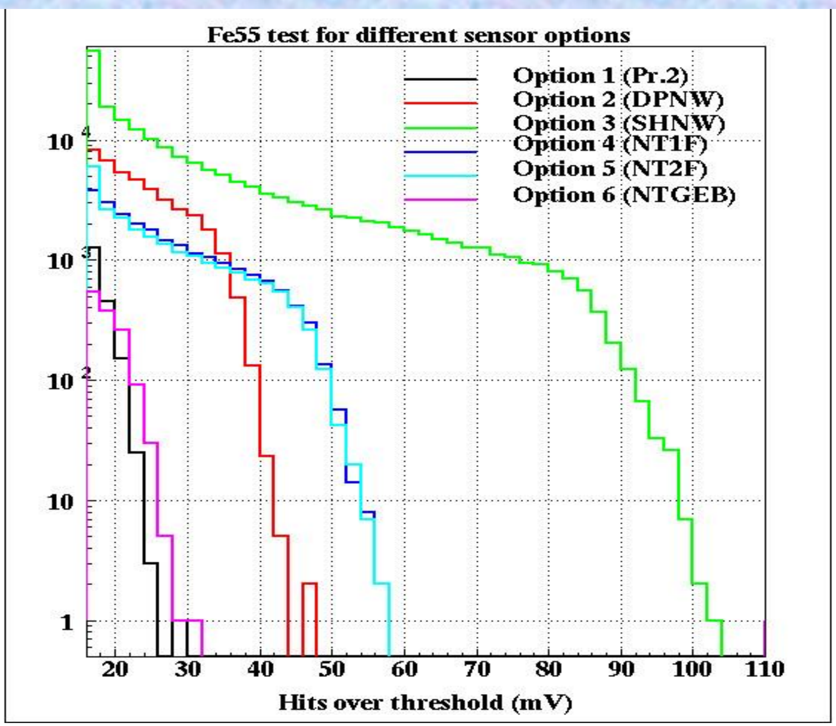
  → Main problem of <u>large sensor capacitance</u> due to 90 nm design rules <u>has been solved</u>

  → 4 out of the 6 options are acceptable for ILC applications (1 – 9.04 fF, 2 – 6.2 fF, 3 – 2.73 fF, 4/5 - 4.9 fF, 6 – 8.9 fF; opt. 1,6 are not accept.)

- ➢ More tests are under way to optimize the design based on minimum ionizing track efficiency.







^{55}Fe results for 6 sensor options:
1 – the same design as prototype 2;
2 & 3 – violate TSMC design rules – granted waiver;
4 & 5 – "natural transistors", allowed by design rules, with gate connected to source and drain;
6 – same, as 5, but gate connected to external bias.

3D Vertical Integrated Circuits (VIP Chip)

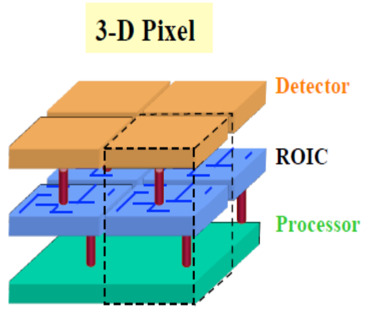
M. Demarteau/
R. Lipton

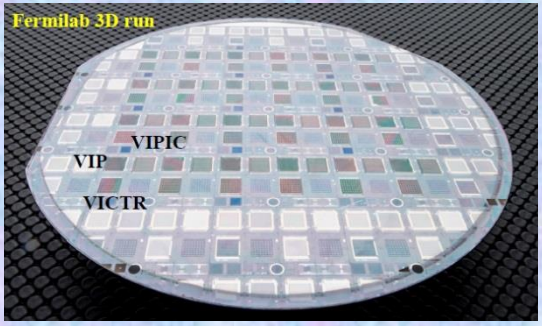
- ➢ An alternative to achieving ultra-low material budget is 3D integrated circuits:

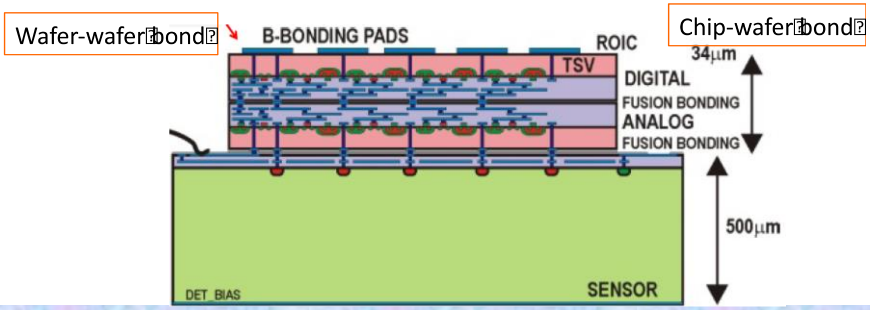
- ❖ Fermilab 3D-IC MPW Run for HEP (2010): 3 chips VICTR(CMS),VIP(ILC),VIPIC(x-ray)

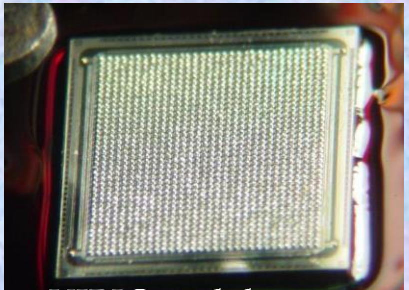
Vertical Integrated pixel (VIP) chip for ILC:
- single pixel time stamping
- 24 x 24 μm^2 pixels, 192x192 array

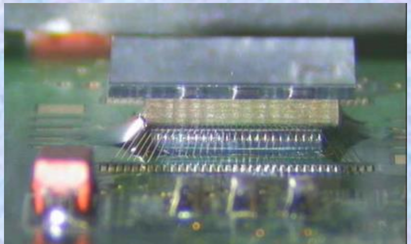
- Two layer 3D ASIC bonded to silicon wafer
- ASIC is thinned to TSV for metal contact to the sensor on other layer of the ASIC
- ASIC is 34 μm thick



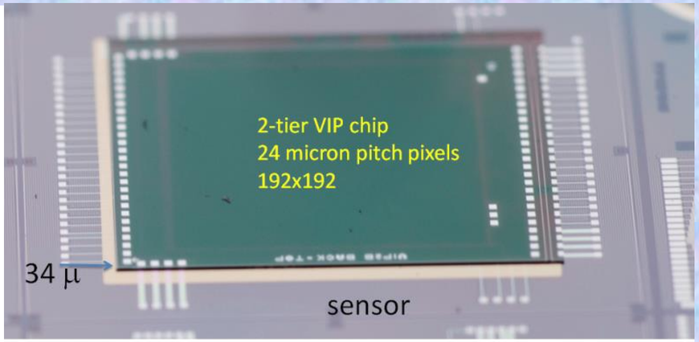





VIPIC with bumps


VICTR with top sensor and interposer

VIP CHIP & TESTING:

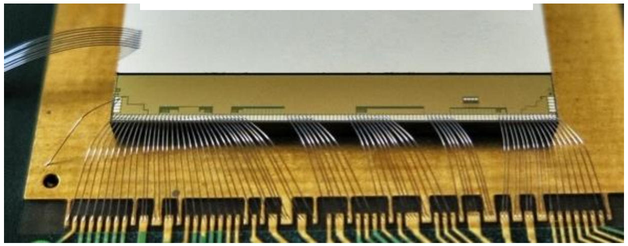


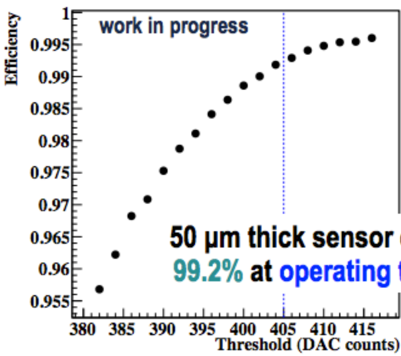
- ➢ Successfully read out all 192x192 = 36,864 pixels
- ➢ Token passes though at 189ps/pixel
- ➢ Sees source
- ➢ Issues with test pulse masking,
- ➢ odd row test pulse
- ➢ Beam test winter 2014

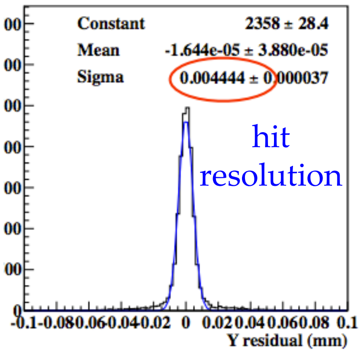
CLIC Vertex Detector R&D

D. Dannheim

Ultra-thin sensors

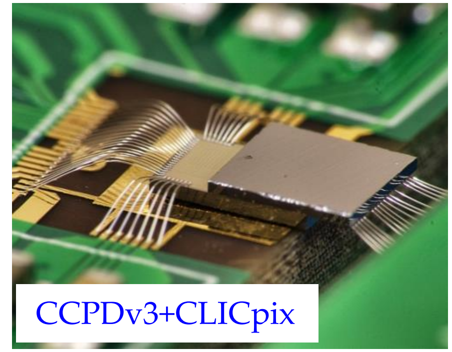


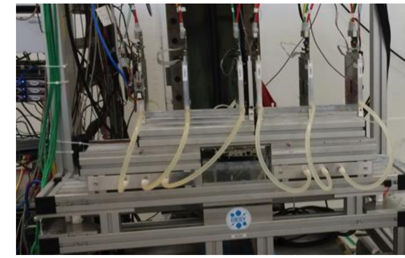




S. Redford, tracking+vtx session Tuesday morning

Test beams with new readout ASICs

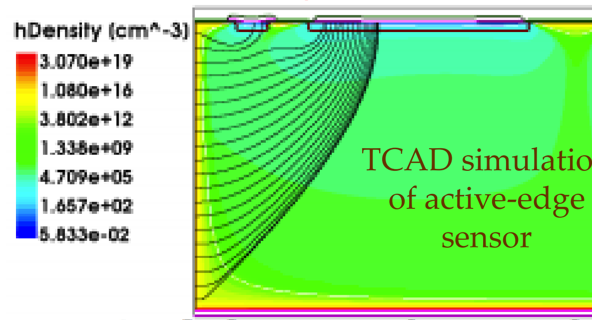


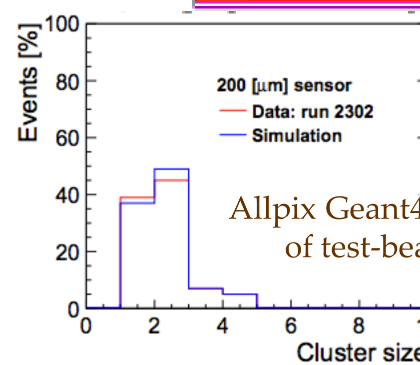


Timepix3 in AIDA telescope (CERN PS-T9)

S. Arfaoui, tracking+vtx session Tuesday morning

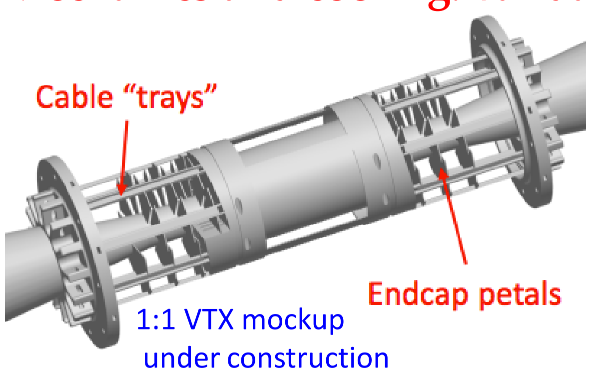
Sensor and r/o simulations

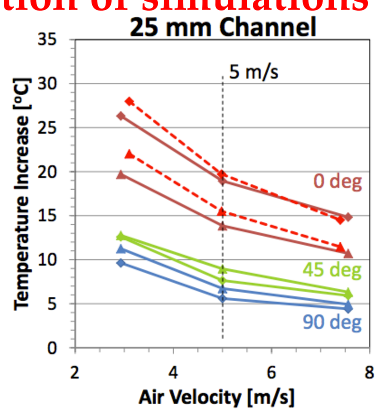




N. A. Tehrani, simul. session Th. afternoon

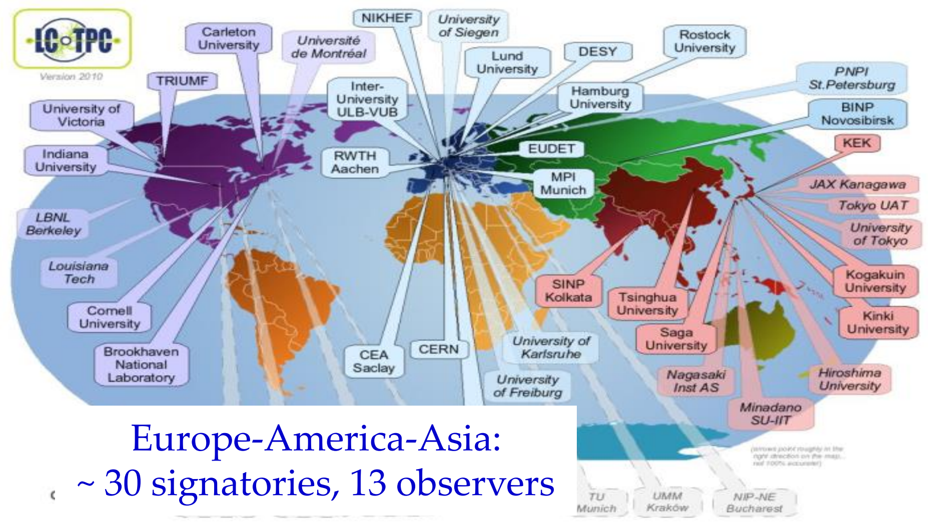
Mechanics and cooling: validation of simulations





F. Duarte-Ramos, tracking+vtx session Thursday afternoon

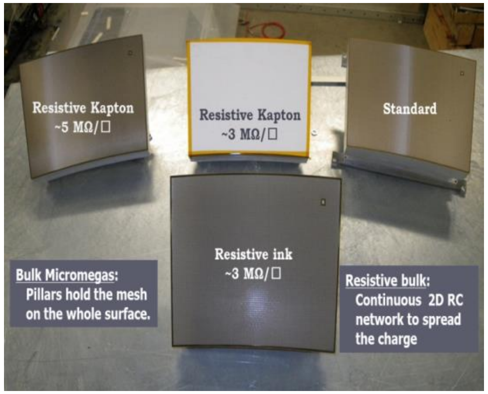
Time Projection Chamber R&D: LCTPC Collaboration



Europe-America-Asia:
~ 30 signatories, 13 observers

TPC with MPGD-Readout
→ spatial resolution < 100 µm @ 4T

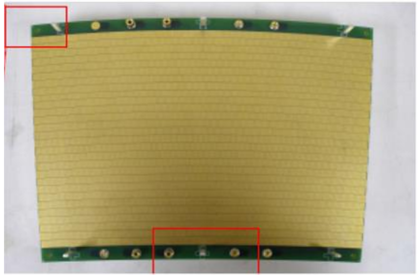
- Wet-etched triple GEMs
- Laser-etched double-GEMs 100µm thick ("Asian")
- Resistive MM with dispersive anode
- InGrid (integrated Micromegas grid with pixel readout); GEM + pixel readout

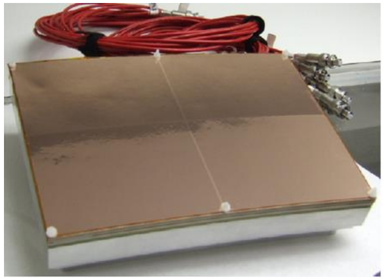


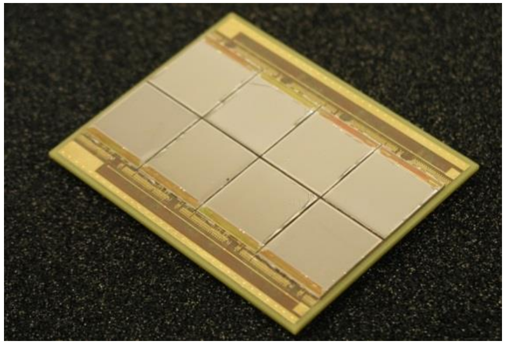
Resistive MM:
CEA Saclay (P. Colas)
Carleton (A. Bellerive)

Laser- etched GEMs: KEK (T. Matsuda, K. Fujii); Univ. Saga (A. Sugiyama)

Wet-etched triple GEM: DESY (T. Behnke) RWTH Aachen (S. Roth)







InGrid: Bonn (J. Kaminski). Saclay (D. Attie), NIKHEF (J. Timmermans); Kyiv (O. Bezhyyko)
GEM-pixel: Bonn; Siegen

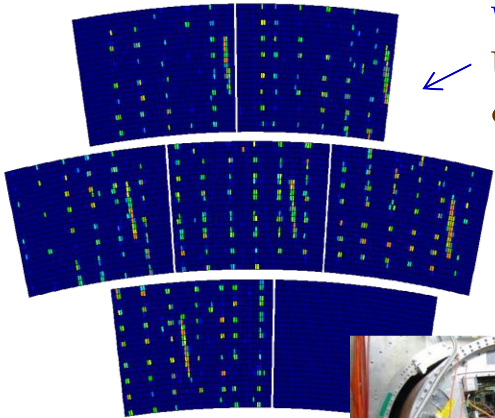
Mechanics – Cornell (D. Peterson); Kansas (G. Wilson); Electronics – L. Jonsson (Lund)

LCTPC R&D: Ongoing Activities

J. Kaminski

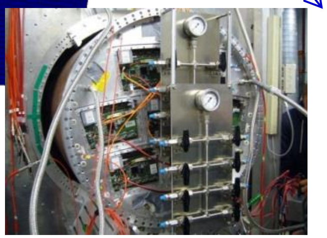
Efforts to improve the modules design for all technologies. Several test beams campaigns:

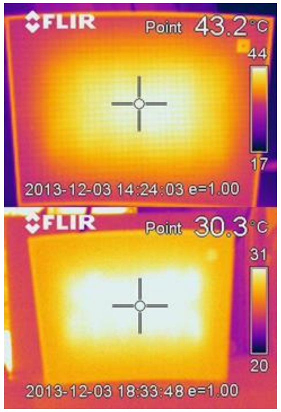
- 7 Micromegas modules with 2-phase C02 cooling

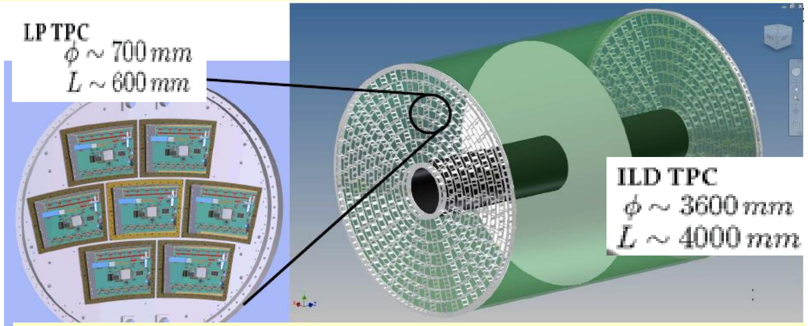


With beam and laser dots:
UV laser gererates MIP tracks & illuminate calibration spots

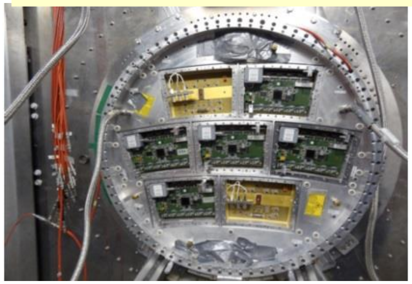
2P CO2 Cooling

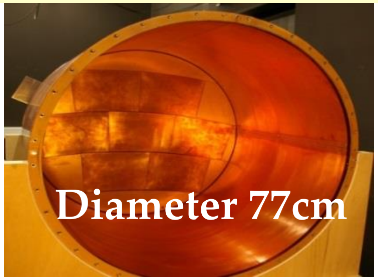




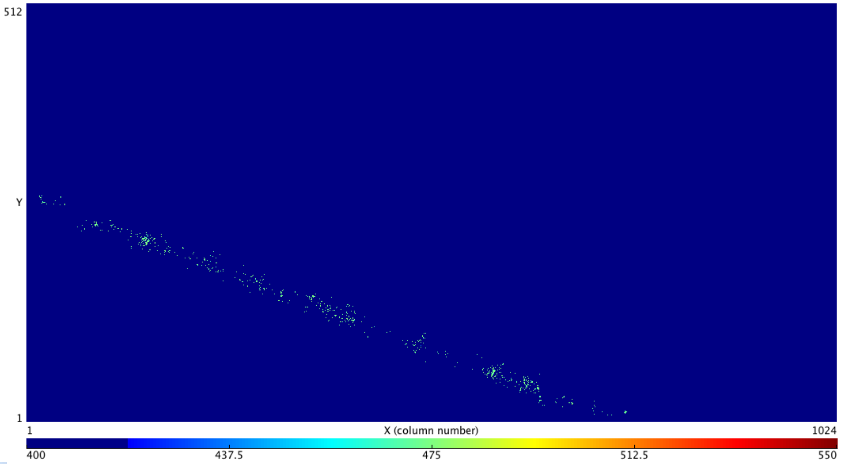


Large TPC Prototype with versatile endplate @ DESY

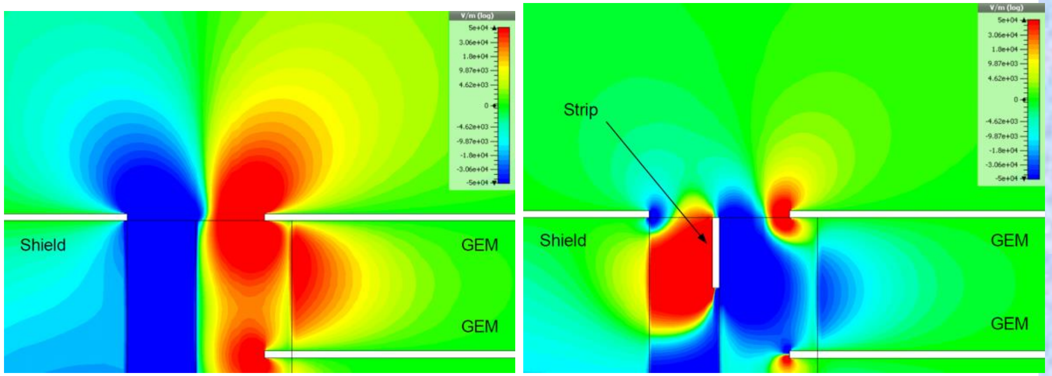




- 5 MM modules and 2 InGrid modules



- 3 Modified GEM Modules
  → Improvement of field distortions between modules by adding a strip

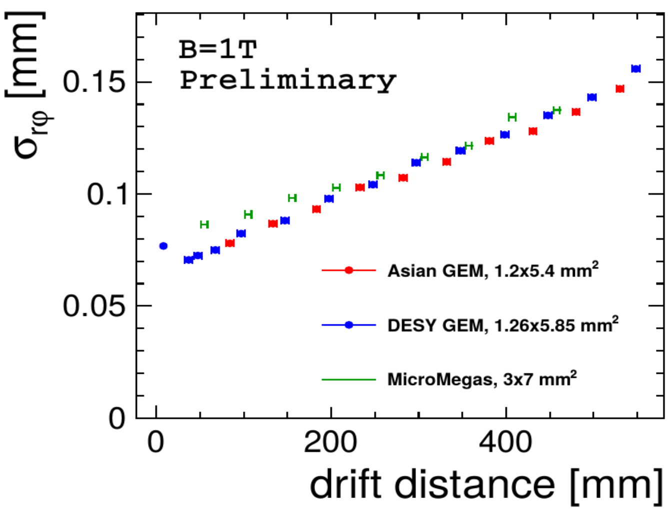


LCTPC R&D: Ongoing Activities

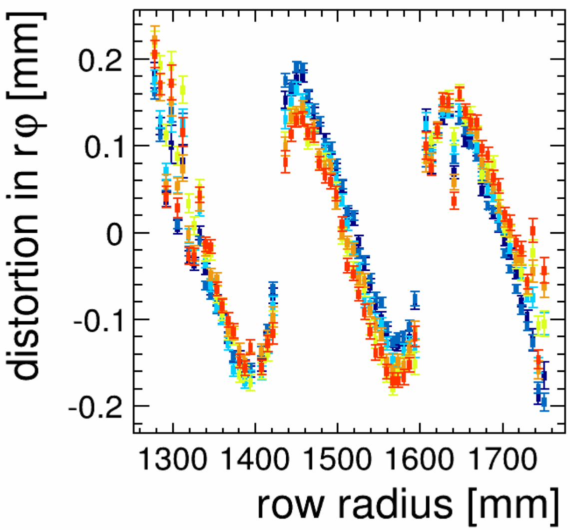
J. Kaminski

❖ Major effort to improve and unify the reconstruction and analysis software:
→ MarlinTPC – for example correction of inter-module field distortions.

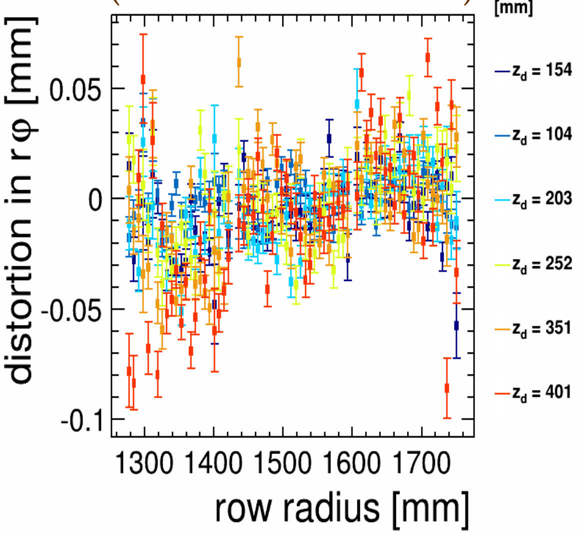
Goal for final TPC can be reached:
GEM / MM performance similar



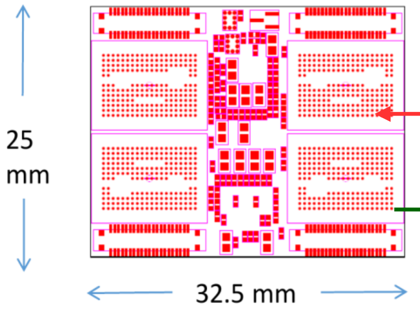
MM (B=0): Before correction

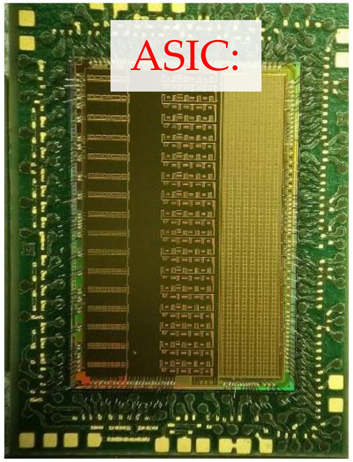


MM (B=0): After correction
(note – different scale)

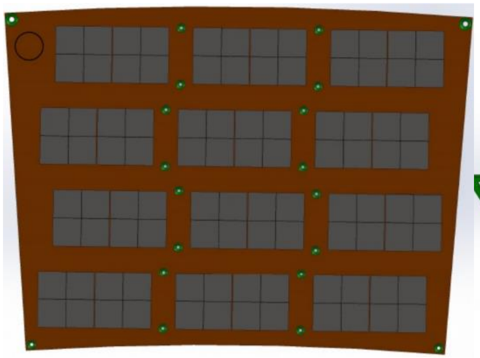


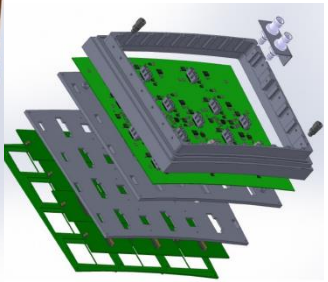
For the close future a new set of electronics based on the SALTRO-16 is in preparation





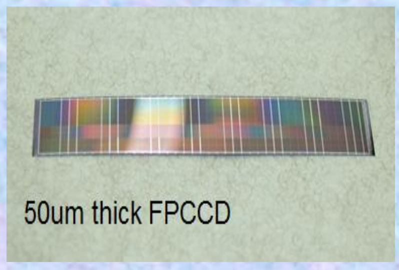
Next Step for InGrid: Develop and equip a Full LCTPC module (~100 chips) @ "InGrid"s

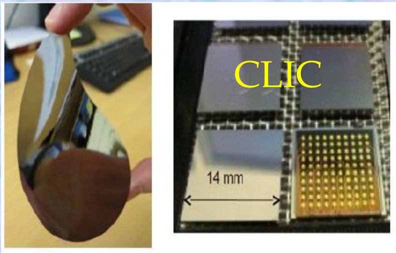


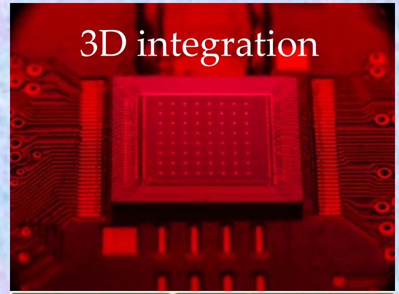


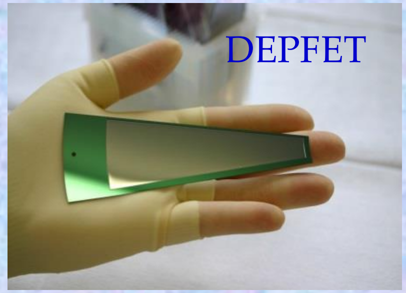
Detector R&D Liason Report: Summary of Contributions

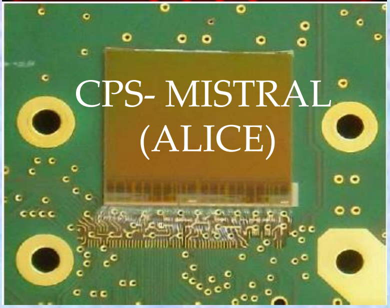
VERTEX	Comments	Status OK ?
CMOS MAPS M. Winter, Strasbourg	Waiting for update	
DEPFET M. Vos, IFIC	Waiting for update	
FPCCD Y. Sugimoto, KEK	OK	
3D-pixel and integration (VIP); R. Lipton, FNAL	OK	
Chronopixel N. Sinev, Univ. Oregon	OK	
SOI, Y. Arai, KEK	OK	
Hybrid Sensor +ASIC; HV-CMOS + ASIC L. Linssen, CERN	Bullet points only; update needed	

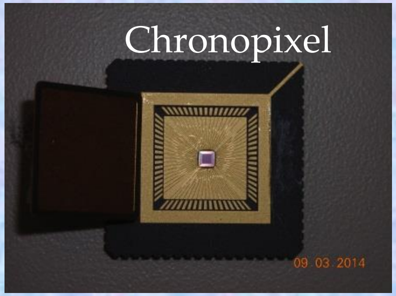


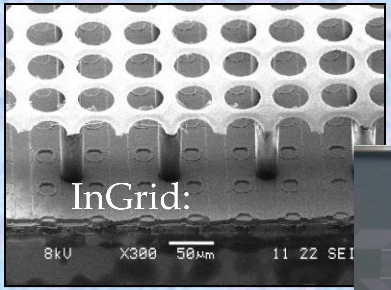


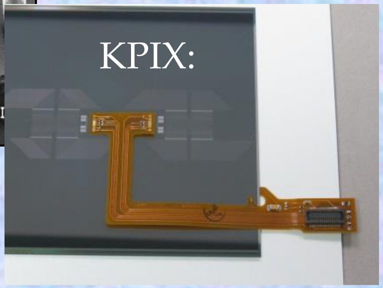












TRACKING	Comments	Status OK ?
TPC (Gaseous Tracking) J. Kaminski, Bonn	TPC ECFA R&D panel need Indiv. group contr.	
LSTFE ASIC (silicon) B. Schumm, SCIPP	Some editing needed	
KPIX ASIC (silicon) M. Breidenbach, SLAC	OK	

Calorimeter R&D: CALICE Collaboration

GOAL:

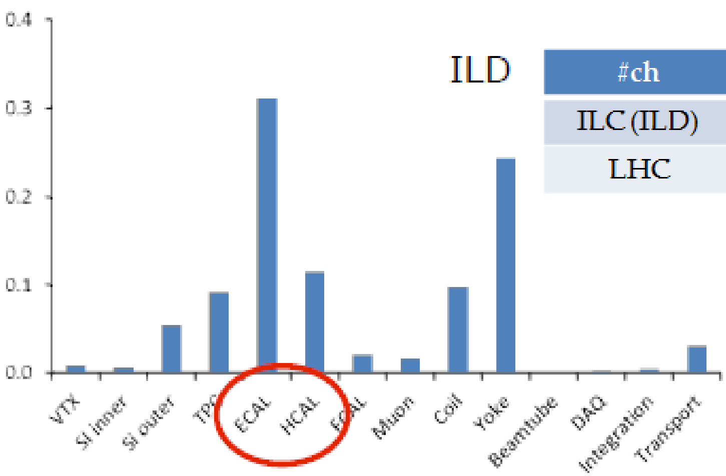
- ❖ Development and study of finely segmented/imaging calorimeters
- ➢ Initially focused on the ILC/CLIC
- ➢ Now widening to include the developments of all imaging calorimeter

2nd largest R&D collaboration in HEP

4 continents
19 countries
59 institutes
361 physicists/ engineers

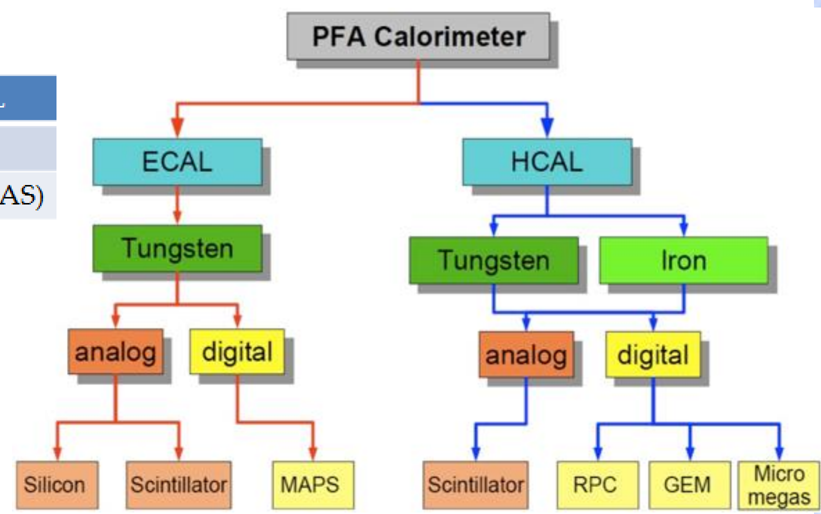
❖ R&D in Calorimetry is an LC driven effort → a marriage with "Particle Flow Algorithm" (pioneering work) has delivered a proof of principle and been established experimentally

Detector cost is driven by instrumented area rather than channel count



#ch	ECAL	HCAL
ILC (ILD)	100M	10M
LHC	76K(CMS)	10K(ATLAS)

ILD/SiD Calorimeter Concepts:



CALICE R&D: Technological Prototypes

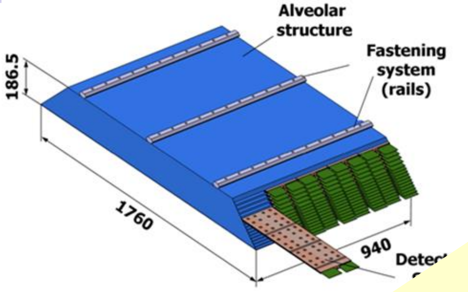
J. Repond

- 1st generation of large prototypes built/tested (SiW ECAL, Sc-W ECAl, Sc-Fe/HCAL,RPC-Fe/W HCAL (mostly without embedded electronics, integrated HV / LV, power pulsing)
- 2nd generation prototypes meant to address all remaining technical issues (sc… able to the size needed for a 4π detector; not necessarily fully instrumented (at this p…

Tests on the bench and in test beams in 2014/5

Silicon – Tungsten ECAL

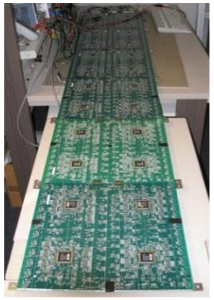
- 5 x 5 mm² pads
- New generation readout (embedded, power pulsing)
- Semi-automated assembly, wedge shaped mech… …cture



Scintillator… …sten ECAL

- Sc… strips with MCCPs (4 x 45 mm²)
- …ation of Split Strip Algorithm → 5 x 5 mm² eff. Gran.
- …ge shaped, same absorber as for SiW
- New generation readout (embedded, power-pulsing

…/W (1st proto with power-pulsing, self-supporting str., compact)



Scintillator – Fe/W HCAL

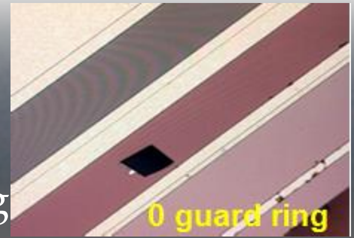
- 3 x 3 cm² scintillator pads
- New generation readout (embedded, power pulsing
- Wedge shaped

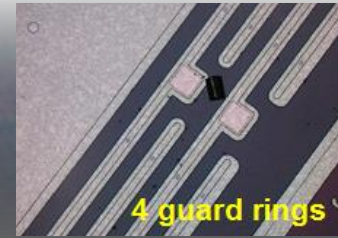
CALICE R&D: Further R&D on Active Elements

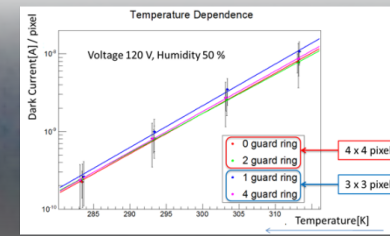
J. Repond

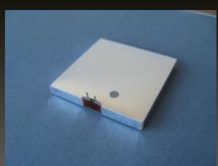
Silicon sensors

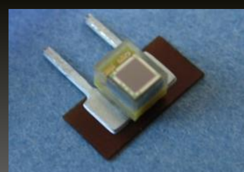
Guard ring design studies
→ segmented or no guard ring











Scintillator pads / strips

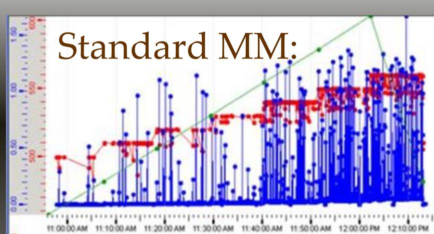
- Tiles with dimples → easier assembly, uniformity
- Wedged tip of strips → more uniform response

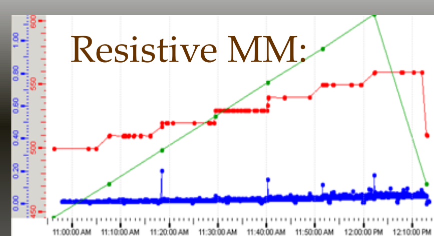
MPPC developments

- Improved linearity, Si-purity; increased # of pixels
- Implement. of barrier (noise rate), trench (cross-talk)

Resistive Plate Chambers (RPCs)

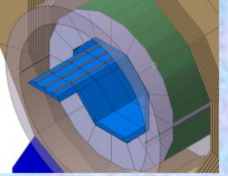
1-glass design → beam tests (successful!)
Development of semi-conductive glass → higher rates





GEM / Thick GEMs / Micromegas

MM: implementation of resistive layer
→ reduced spark rate



Silicon-Tungsten (SiW) ILD ECAL

V. Balagura

Kyushu, Tokyo Uni., LLR, LAL, LPNHE, LPSC

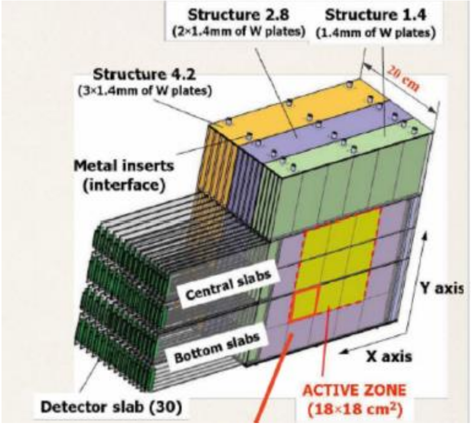
SiW ECAL: Low systematics → Perfect linearity, simple calibration, stable in time, robust
Cost reduction → 10% of bad pixels is affordable (not tracker device)

1st Physical Prototype (2005-2011):

Conceptual proof of PFA, verification of MC

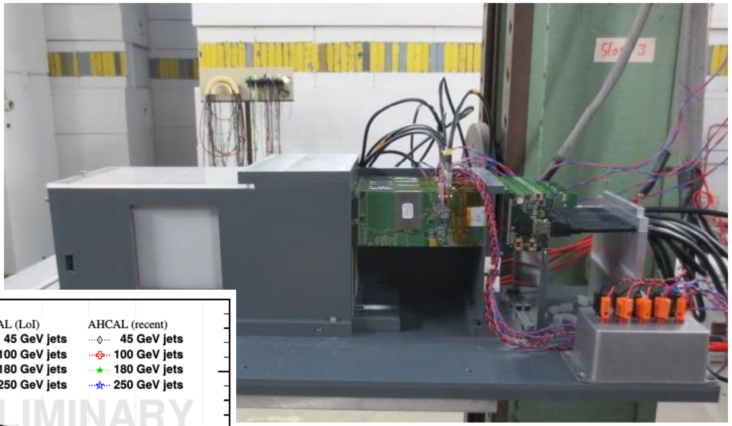
10x10 mm2, 30 layers
Electronics outside

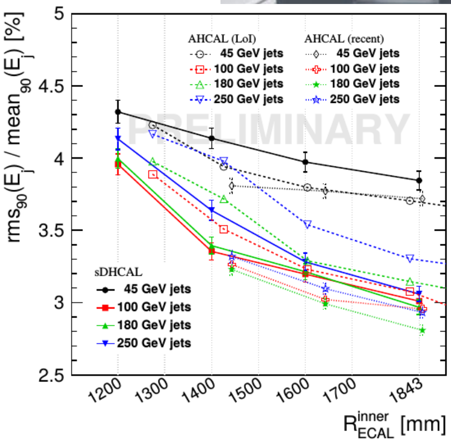
$\sigma E/E = 16.6\%/\sqrt{E} \oplus 1.1\%$,
linearity within 1%.



2nd Technological Prototype (2012-present)

- Embedded electronics
- Choice and finalize design
- Prepare mass production





Optimize performance vs cost as a function of ILD dimensions,

BROADENING THE SCOPE:

Recent interest to SiW(Pb) technology for :

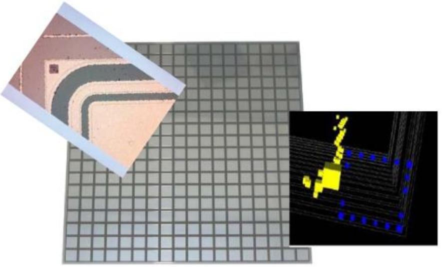
- CMS endcap Phase 2 upgrade (HGCAL)
- Future circular colliders (TLEP, CEPC).

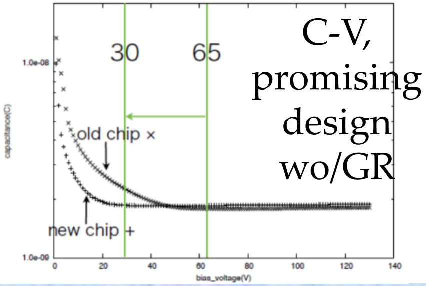
Silicon-Tungsten (SiW) ILD ECAL: Ongoing R&D

V. Balagura

Silicon sensors

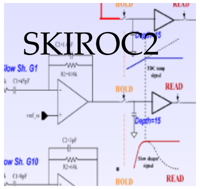
- R&D in Hamamatsu HPK (CNRS, Kyushu)
  →2.5 EUR/cm2; know-how design :"no guard ring"
- LFoundry (Europe) with CNRS
  →Larger (8') and thicker (700 um) sensors.

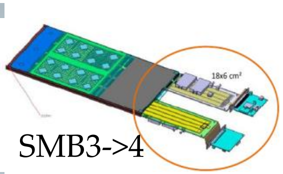




DAQ electronics

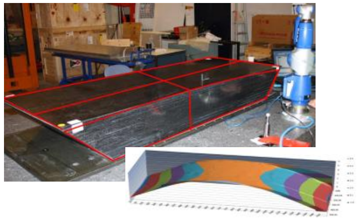
→FE chip SKIROC2, new production in fall 2014
→ 2 new PCBs, produced, partially tested
→ test board for FE chip is being designed

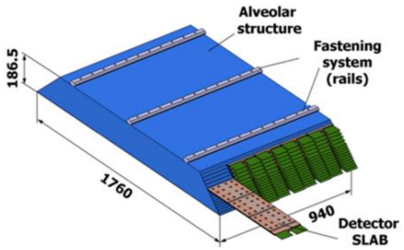




. Mechanics

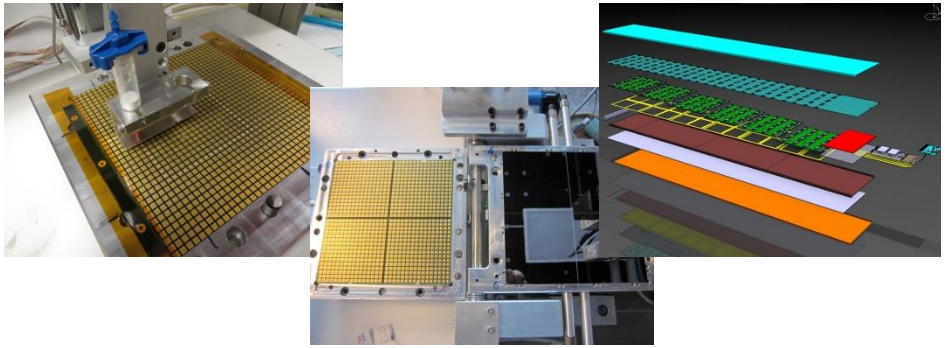
→ 3/5 x ILD barrel module (600 kg, 5 years R&D)
→ verification of simulation results with molded Bragg grating fibers





Detector assembly

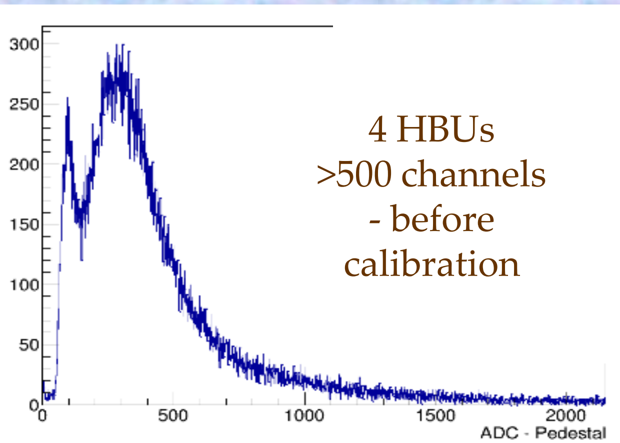
→ 9 sensors successfully glued by robot
→ next: glue 4 sensors per PCB, tested with glass plates
→ quality assurance documents for each detector are being prepared

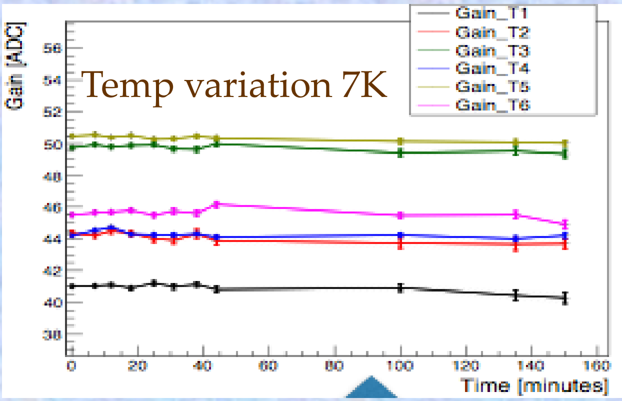


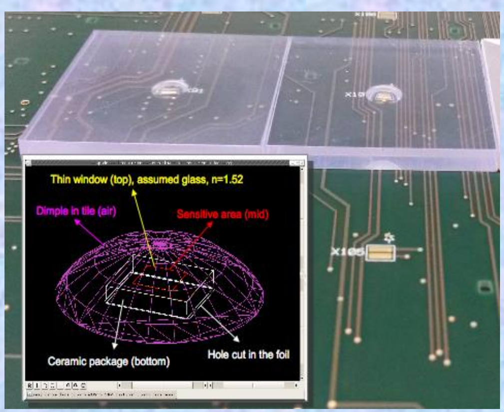
AHCAL R&D: The Scintillator Analogue HCAL

F. Sefkow

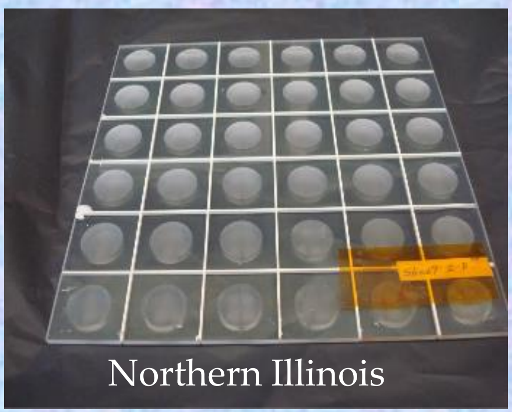
- **SiPM trends:** driven by industry, medical applications: benefits in present prototype
  - uniformity → simplification: no need anymore for light yield, gain and threshold equalisation
  - lower noise → higher over-voltage → better T stability
- **Scintillator trends:** optical coupling concepts amenable to mass production - under test in present prototype
  - No WLS fibre (blue-sensitive sensors), SiPM on board, mega-tiles



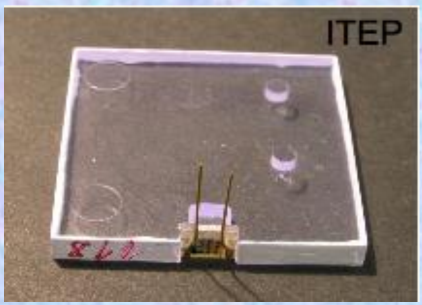




Mainz, with DESY und Uni HH



Hamamatsu sensors, on or in PCB surface



CPTA, KETEK or Hamamatsu sensors no WLS fibre

individually wrapped; KETEK sensors

AHCAL R&D: The Scintillator Analogue HCAL

F. Sefkow

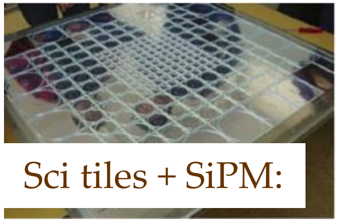
Flexible Test-Beam Roadmap towards 2nd generation prototype (synergy with ScECAL):

- General approach: proceed with system integration whilst remaining open on sensor technology side
  → possible thanks to versatile electronics

- 2014 (ongoing at CERN PS) → 3 ECAL + 24 HCAL units = shower start finder + 4 big layers (~ 4000 channels); Fe and W absorbers

- 2015 apply for SPS → same configuration

Large Scale Prototypes:

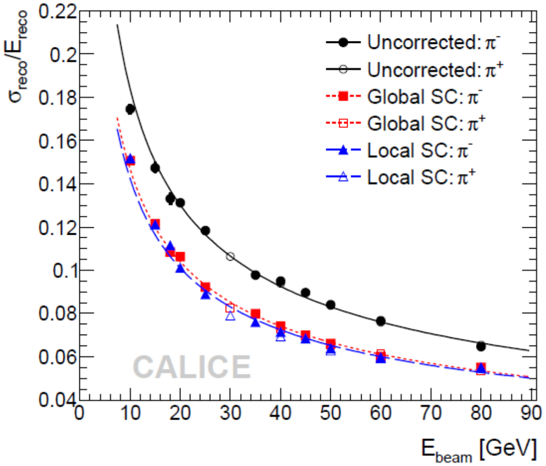


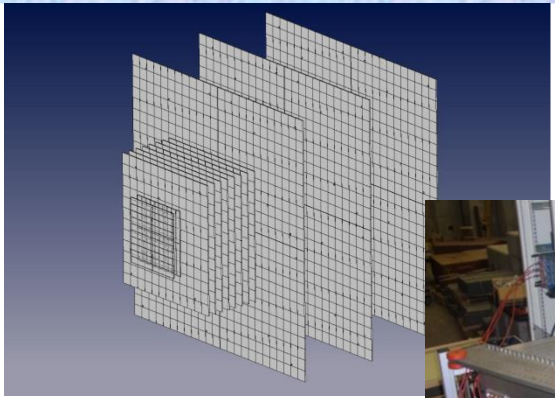
Sci tiles + SiPM:

$1m^3$ abs.: steel or W

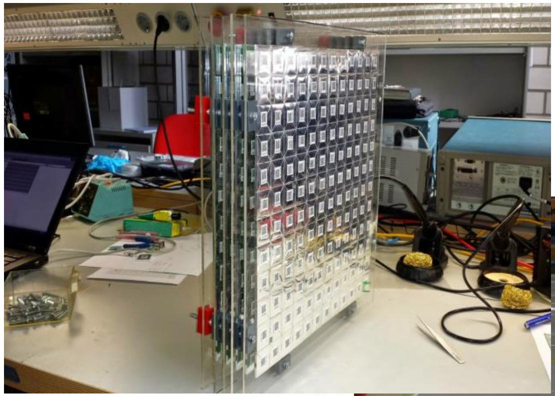
Earlier AHCAL test-beam:

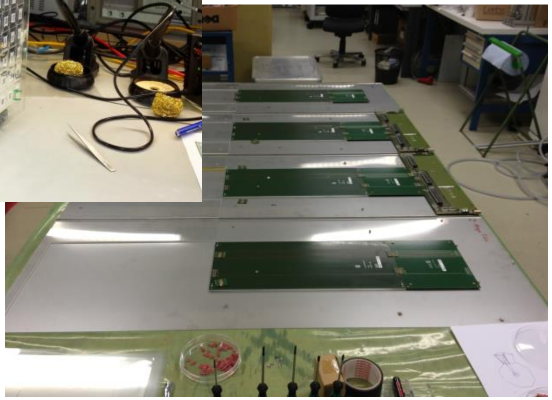
Excellent hadronic energy resolution by software compensation





Test beam at CERN PS in Oct and Nov/Dec 2014





SDHCAL R&D: RPC for HCAL

I. Laktineh

First technological ILC prototype :

- Ultra-granular, power-pulsed, compact
- Self-supporting mechanical structure.
  - → 10500 ASIC were calibrated
  - → 310 PCBs were produced
  - → 50 detectors were assembled (at CERN) with their electronics into cassettes

Next steps:

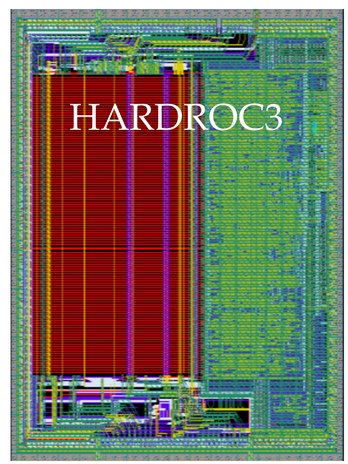
→ 3rd generation HARDROC3 tested (power-pulsed, zero-suppress, I2C); large dynamic (up to 50 pC)

→ Large GRPC with optimized gas irrigation system are being produced

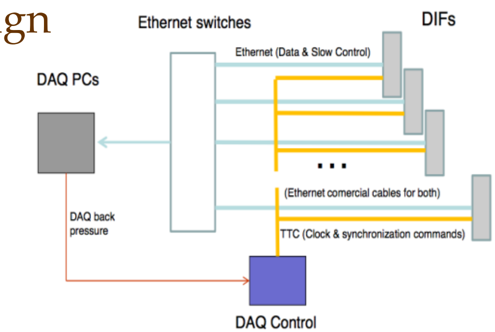
→ Large electronic board are being conceived to equip the large chambers

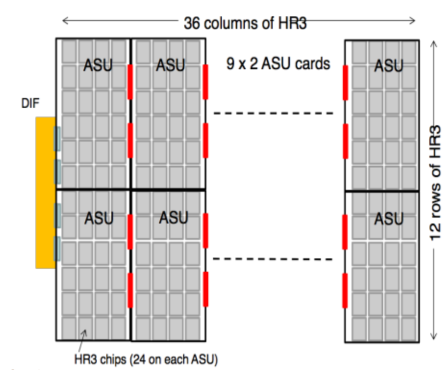
→ New DAQ using LHC stanadards are being conceived

→ A prototype of 4 large (2 m^2) instrumented detectors will be built in 2015-2016



New DAQ design





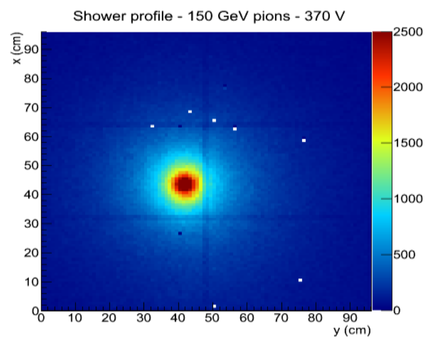
New ASU design

SDHCAL R&D: Micromegas for HCAL

M. Chefdeville

Large-area prototypes of 1x1 m² with embedded front-end electronics : NIMA729 (2013) 90 , A763 (2014) 221

- Micromegas with 1 x 1 cm2 pads
  → ~37,000 readout channels
- Interspersed in RPC-SDHCAL
  (use SDHCAL to reconstruct shower start!)



2014-2015: Development of spark protection using resistive films LC (SDHCAL) and HL-LHC

Goal : Suppress spark (and deadtime) and maintain high-rate capability, linearity

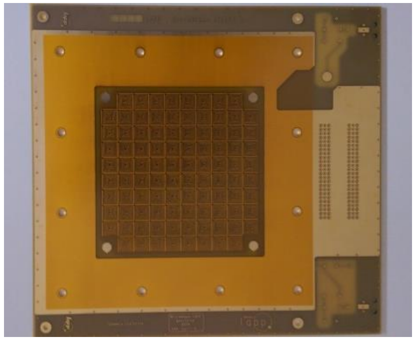
How: Systematic study of small prototypes with different resistive films

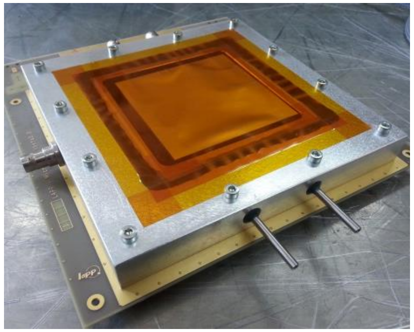
Status : Prototype fabrication on-going (stack of 10)

Test program: dE/dX scan with 55Fe source & GEM injector + Rate scan with X-ray gun ;

Testbeam: pion-electron showers in November 2014 (SPS : energy & rate scan)

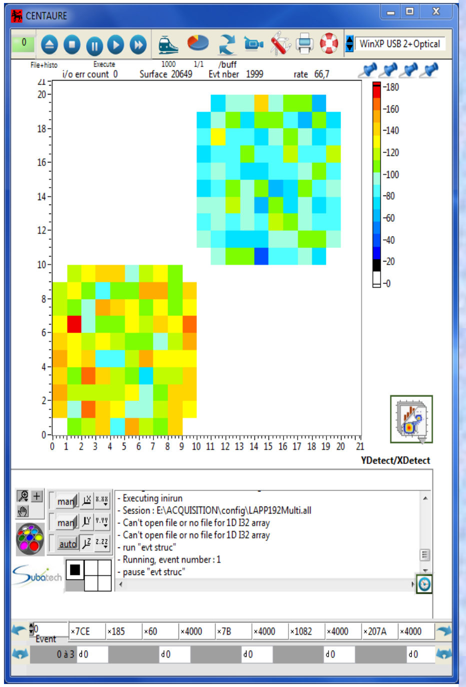
PCB with pads & resistive pattern





Chamber for X-ray tests

DAQ ready



GEANT4 and CALICE

J. Repond

❖ **In the past**

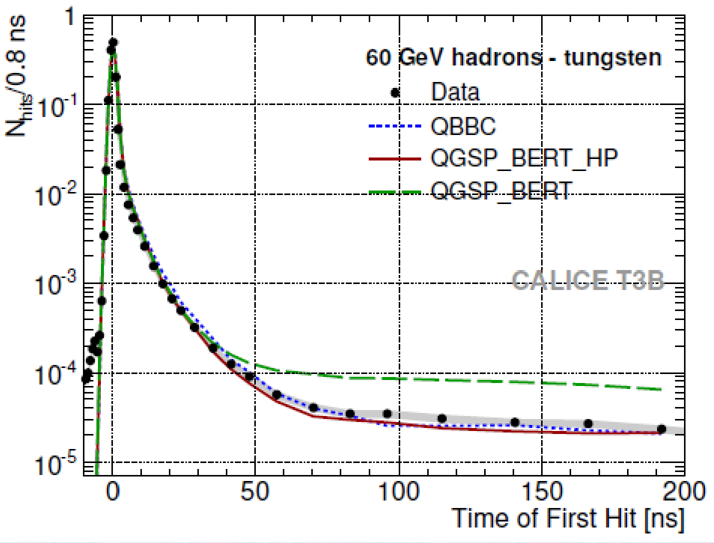
➢ Detailed comparisons of CALICE data and GEANT4-based predictions

❖ **On September 18th**

First common GEANT4 and CALICE workshop

- Well attended with ~25 participants
- Discussion of implementation of history of showers
- Discussion of photon-production cross sections
- Discussion of features in most recent releases (GEANT10.x)

Id	parent	type	First Secondary	Next Sibling
1	-	p	2	-
2	1	e-	7	3
3	1	e-	-	4
4	1	pi	-	5
5	1	n	-	6
6	1	p	-	-
7	2	g	-	8
8	2	e-	-	-



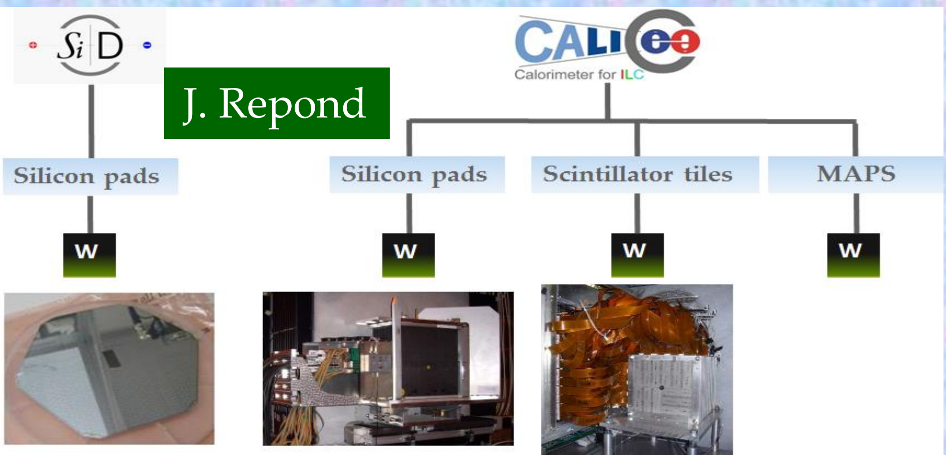
GEANT4 benefits from CALICE measurements

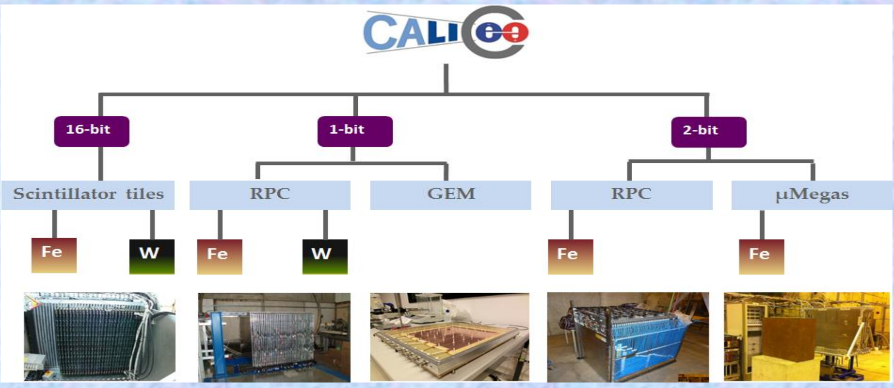
➢ Test beam results not used for tuning
➢ Used as an important cross check
➢ CALICE data unique in this respect

SOFTWARE IN THE DETECTOR R&D LIAISON REPORT

Detector R&D Liason Report: ECAL and HCAL Contributions

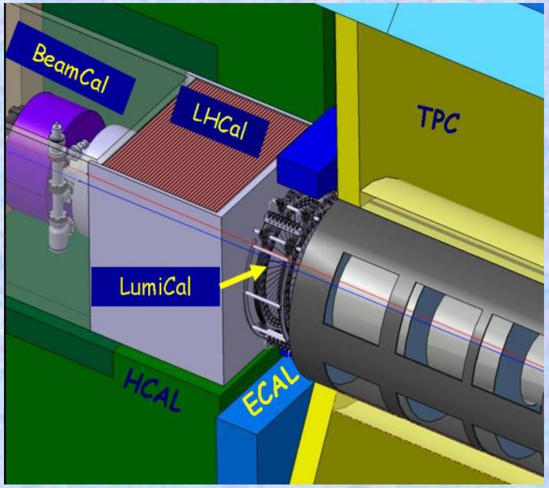
ECAL	Comments	Status OK ?
Sci. ECAL T. Takeshita, Shinshu	Being improved	
Si–W ECAL(ILD): K. Kawagoe, Kyushu V. Boudry, LLR, R. Poeschl, LAL	OK	
Si-W ECAL (SiD) M. Breidenbach, SNAL	OK (engineering)	
Si-W ECAL (SiD) D. Strom, Univ. Oregon	pending	
TPAC MAPS	CALICE report	No active contact

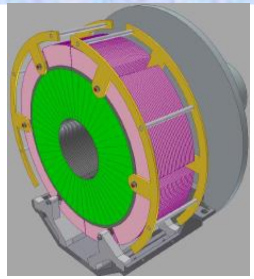




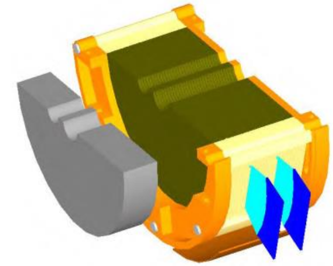
HCAL	Comments	Status OK ?
SDHCAL I. Laktineh, Lyon	Engineering section being expanded	
Sci. HCAL F. Sefkow, DESY	OK	
RPC DHCAL J. Repond, ANL	OK	
GEM DHCAL A. White, UTA	Issues being addressed	
MM SDHCAL M. Chefdeville, LAPP	OK	
Dual Readout J. Hauptman, Iowa State	OK	

Forward Calorimetry R&D: FCAL Collaboration





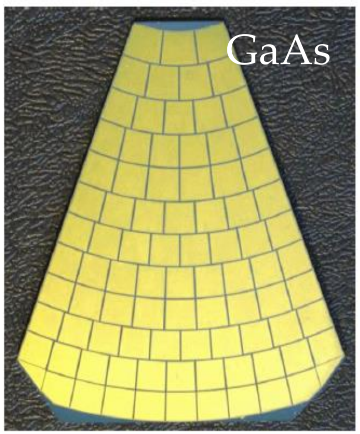
LumiCal:
→ precise luminosity measurement
10^{-3} - 500 GeV @ ILC
10^{-2} - 3 TeV @ CLIC



BeamCal:
→ inst. lumi measurement / beam tuning, beam diagnostics

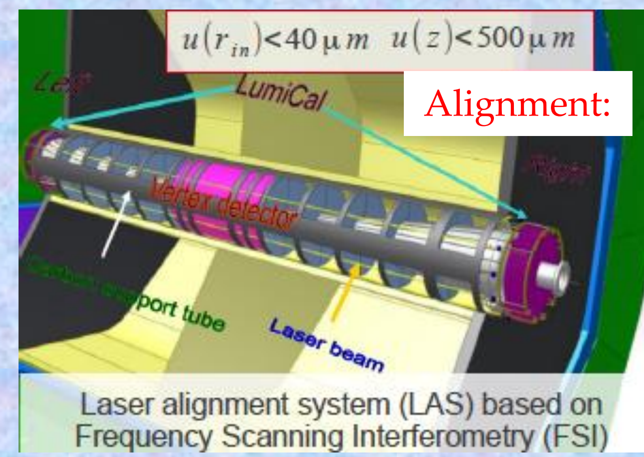
LumiCal: Two Si-W sandwich EM calo at a ~ 2.5 m from the IP (both sides)
30 / 40 (ILC/CLIC) tungsten disks of 3.5 mm thickness
BeamCal: very high radiation load (up to 1MGy/ year) → similar W-absorber, but radiation hard sensors (GaAs, CVD diamond)

BeamCal Sensors



LumiCal ASIC:

Alignment:



- Unique contributions to the ILC DBD, the CLIC CDR, and to the detector concepts ILD and SiD
- Successful prototyping and test of major components in the beam → final preparation of a 'large testbeam paper' (2010 - 2012 results) → the performance of fully assembled sensor planes matches the requirements

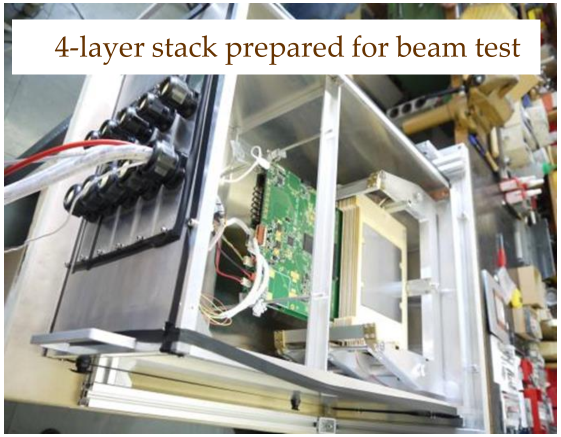
FCAL	Comments	Response OK ?
LumiCal / BeamCal W.Lohmann DESY	Minor editing	

FCAL R&D: Ongoing Activities

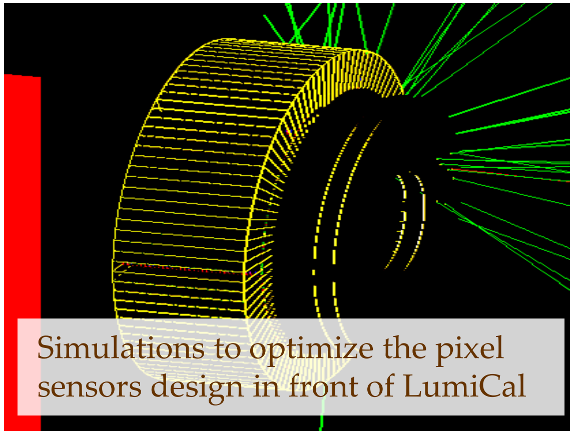
W. Lohmann

Test-beam end of October at CERN:

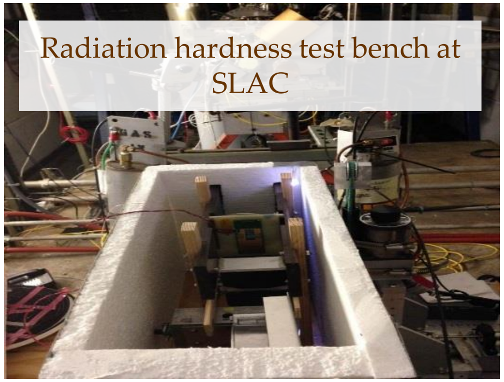
- Four sensor layers assembled with ASICs in a 10 GeV mixed beam
- Acquire expertise to operate a multi-layer structure
- Data-MC comparison



4-layer stack prepared for beam test



Simulations to optimize the pixel sensors design in front of LumiCal



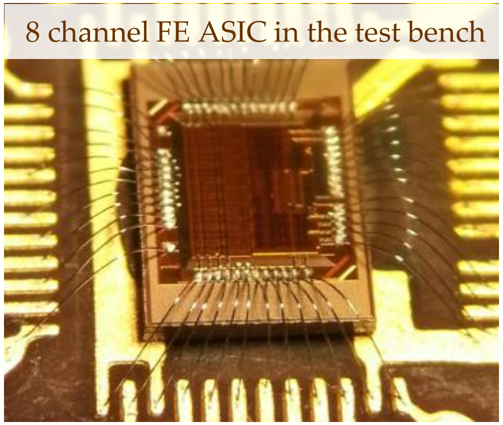
Radiation hardness test bench at SLAC

Sensor R&D:

- Pixel sensors in front of LumiCal (improve shower position reconstruction, alignment)
- Edgeless sensors for LumiCal (to reduce dead areas)
- Radiation hardness studies in a ‘realistic’ environment (T506 at SLAC) of the Si and GaAs sensors

ASIC development (130 nm CMOS):

- 8 channel FE ASIC, dual gain, low power consumption; 8 channel SAR ADC
- Prototypes of both ASICs are tested and match the specification
- Power pulsing implemented
- Next step will be to enhance the number of channels per chip, integrate in a readout board



8 channel FE ASIC in the test bench

Summary and Outlook

- Linear Collider R&D remains a very active field
  → synergies exists with other projects HL-LHC, STAR, ALICE, Belle2, …
  → important to keep an eye on new technologies, since the existing designs were started a long time ago

- The COMMUNITY SUPPORT is a KEY for the Detector R&D Liaisons:
  → compiling an overview of the detector R&D field is a lot of work and cannot happen without YOUR help

- We would also like to thank to the LC Community for your contributions !!!
  → ALL GROUPS (which were contacted on a short notice) sent inputs to this talk !

Thank you for your help with this effort so far.
The Detector R&D Liaison Report is getting its final shape → first draft to be send to the different R&Ds collaborations shortly after LCWS