ILC Detector R&D:

Report from R&D Liaisons & French contributions

LCCPDeb
Detector R&D Liaisons:

Jan Strube (PNNL)
Maxim Titov (CEA Saclay)

4èmes Journées Collisionneur Linéaire,
Paris, France,
March 23-24, 2016

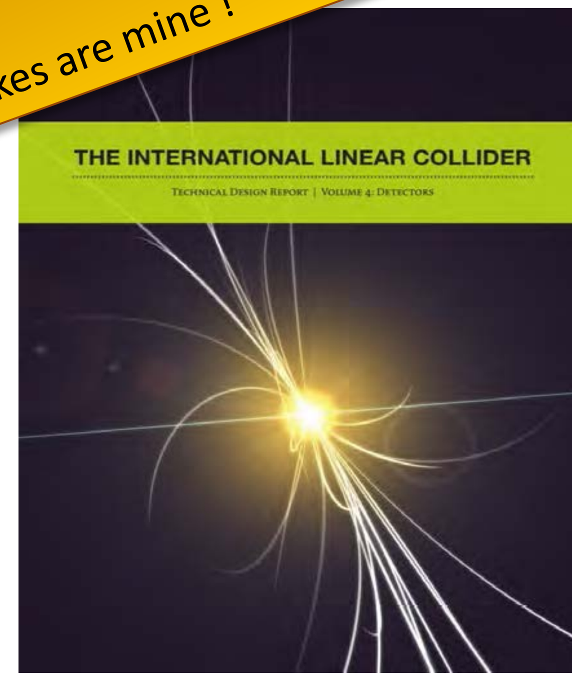
ILC Detector R&D: French Landscape

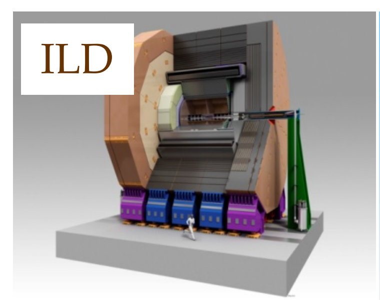
June 2013: Detailed Baseline Design (DBD) for Detectors
http://www.linearcollider.org/ILC/Publications/Technical-Design-Report

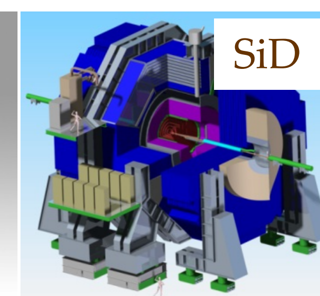
❖ The ILC DBD is NOT a Detector TDR
→ missing detailed engineering; ILD/SiD optimization

❖ Not all R&D has been completed → R&D remains an ...

"Push-pull Option" – 2 det...rs:
similar co...
diffe...
(ce... ...C)
...n choices







Many thanks to everyone who contributed to this talk and the R&D Liaison Document

Challenging to summarize → all mistakes are mine !

This talk concentrates on detector R&D ef...
Concepts), with emphasize on Fr...

IN2P3 CCL Con...
LLR: Vin... ...ent
LPSC: Jea...
LPNHE: D... ...al
IPHC: Marc ...inter
LPSC Grenoble: Jean-Yves Hostachy
LPC Clermont: Pascal Gay
LAL: Roman Poeschl
LAPP: Max Chefdeville
IPNL: Imad Laktineh
CPPM: Eric Kajfasz

OMEGA: Christophe de La Taille

Irfu/ SPP: Paul Colas

RPC DHCAL

Scintillator ECAL

Collaborations

FCAL

CLICPix

SPiDeR

DEPFET

LCTPC

SOI

ChronoPixel

SDHCAL

LC TPC

TPAC

RPC Muon

GEM DHCAL

KPIX

Silicon ECAL (SiD)

VIP

Silicon ECAL (ILD)

Dual Readout

CMOS MAPS

DEPFET Active Pixel Detector

CALICE Calorimeter for ILC

FPCCD

FCAL Collaboration High precision design

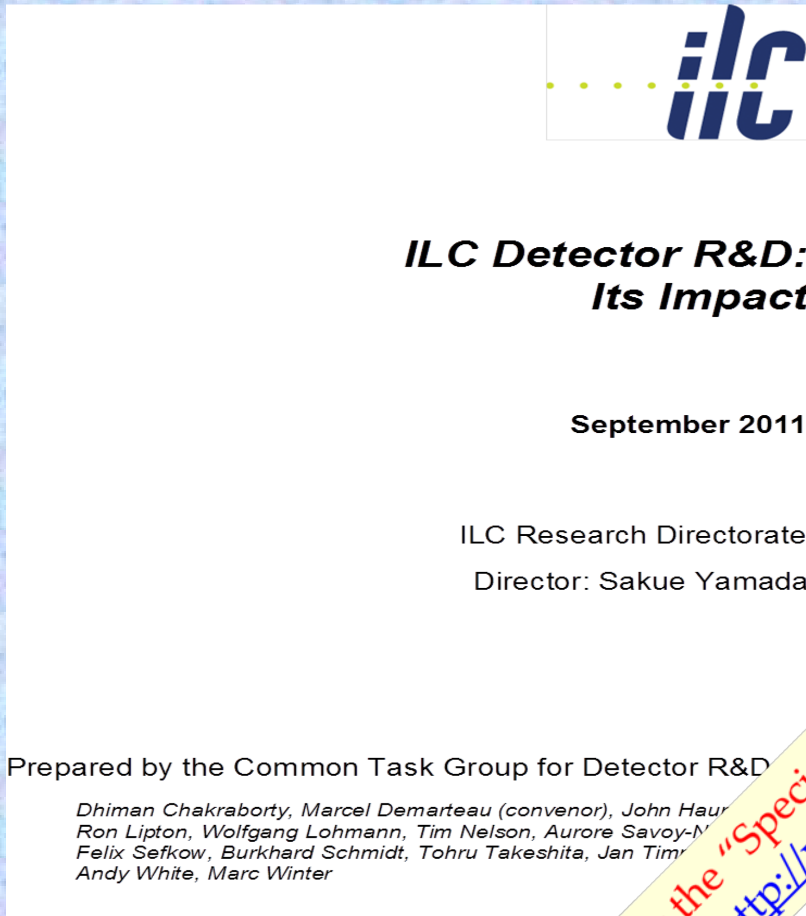
Scintillator HCAL

Many forms of Detector R&D relevant to LC:

- Large collaborations such as CALICE,LCTPC,FCAL
- Collection of many efforts such as the vertex R&Ds
- Individual group R&D activities
- Efforts currently not directly included in the concept groups (ILD, SiD, CLIC), which may become important for LC in future

NB: incomplete list. For illustration purposes only.

ILC Detector R&D: Spin-Offs is a Key Word to Survive


ILC Detector R&D:
Its Impact

September 2011

ILC Research Directorate

Director: Sakue Yamada

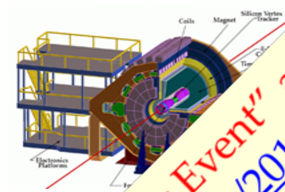
Prepared by the Common Task Group for Detector R&D

Dhiman Chakraborty, Marcel Demarteau (convenor), John Haur… Ron Lipton, Wolfgang Lohmann, Tim Nelson, Aurore Savoy-N… Felix Sefkow, Burkhard Schmidt, Tohru Takeshita, Jan Tim… Andy White, Marc Winter

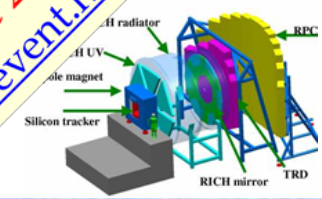
Major Impact in HEP Doma… Beyond ILC:

CMOS-MAPS Initial Objective: IL… …aged performance)
→ applied to hadron experime… …ntermediate requirements (STAR, ALICE…

STAR 2012
Solenoidal Tracker @ RHIC (~ 1600 cm2)



…17 … Baryonic … (~ 500 cm2)



ALICE 2018
A Large Ion Colliderr (Inner Tracker System):

DEPFET for Belle II

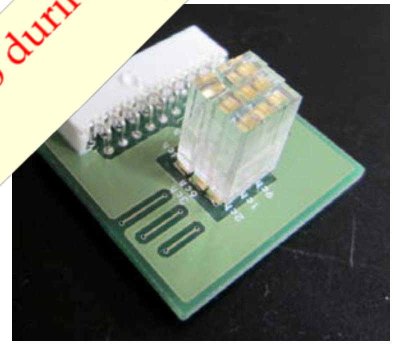
CMOS MAPS for STAR

Also during the "Special Linear Collider Event" at the 2012 IEEE NSS/MIC:
http://www.desy.de/~nss2012/2012LCevent.html

… Outside High Energy Physics:

Prototype for PET Applicatio…

3x3 array of LYS… crystals with SiPMs (300 ps time resolution):



TRECAM (Tumor Resection CAMera): miniaturized gamma-camera for breast cancer surgery

49 x 49 mm² field of view
$LaBr_3$:Ce crystal optically coupled to a multi-anode photomultiplier tube

Detector R&D Liaison Report

LCC PHYSICS AND DETECTORS EXECUTIVE BOARD:
→LC DETECTOR R&D LIAISONS: Maxim Titov (Liaison), Jan Strube (Deputy Liaison)

CHARGE:

- The detector R&D liaison ensures productive communication between the LCC Physics and Detectors Executive Board and detector R&D groups. The liaison is a member of the Executive Board and communicates relevant information from the Executive Board to detector R&D groups and vice versa.

- The liaison is in contact with all detector R&D groups relevant to linear colliders to keep track of the overall detector R&D efforts conducted or planned for linear colliders and to periodically compile summaries of the efforts.

Detector R&D Liaison Report: get an overview over the LC Detector R&D Efforts

- Update of the R&D developments since ILC DBD and CLIC CDR
- "Publicize" the technology. Summarize contributions of individual R&D efforts.
  → Make areas of overlap obvious without pointing out (not an attempt to control R&D groups)
- Provide a "showcase" for the technology. Manpower and financial resources are explicitly not mentioned in the report.
- Provide an entry point for new groups →help them to learn the current landscape of the LC R&D efforts and the areas where they can contribute

Detector R&D Liaison Report

Individual ILC / CLIC R&D Groups were asked to provide a few pages summary (5 questions):

- Introduction. Brief overview of the technology (past R&D efforts with references)
- Recent developments since ILC DBD / CLIC CDR (to avoid receiving historical data);
- Engineering challenges (for putting the technology into a real-world LC detector)
- Future Detector R&D activities in the years to come.
  List of collaborating institutes (contributing to the given R&D technology)
- Application of the R&D outside of LC (with references, if technology is already used)

… and were asked to summarize major activities in the table:

R&D Technology	Participating Institutes	Description / Concept	Achieved Results / Milestones :	Future Activities :

- ❖ Concentrate on the R&D activities for the detector concepts
- ❖ Group individual R&D based on vertexing, tracking, calorimetry, muon , softwware

Detector R&D Liaison Report

- > ~ 50 individuals R&D groups contacted
- List of responses was rather variable → from pointers to past publications to 100+ page documents; from text in the mail to bullet points and to 18+ dedicated pages
- Today: Detector R&D Liaison Report is being written in LaTeX.
  → Currently 140 pages + > 10 pages references.

❖ Separate Chapter - ILC Detector R&D Spin-Offs (not comprehensive one)

Detector R&D Report

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Maxim Titov maxim.titov@cea.fr

Contents

ILC Detector R&D Liaison report structure:
- Motivation and Constraints of the sub-detector in a Linear Collider
- Write-up for each technology
- Summary table
- Executive Summary

Detector R&D Liaison Report: Summary Tables

Vertex Detectors R&D Summary Table:

R&D Technology	Participating Institutes	Description / Concept	Milestones	Future Activities
ChronoPix	University of Oregon Yale University Sarnoff Corporation	ChronoPix is a monolithic CMOS pixelated sensor with the ability to record up to two time stamps per pixel during the bunch train. Hits are read out in the time between bunches.	April 2014: Device tests of prototype 2 inform the design of prototype 3 to be submitted to foundry	Prototype 3 was manufactured in September 2014. Tests have shown that problems revealed in prototype 2 were solved.
CMOS MAPS	IPHC Strasbourg DESY, Hamburg University of Bristol University of Frankfurt	The CMOS pixel sensor uses as a sensitive volume the 10–20 µm thin high-resistivity epitaxial Si-layer deposited on low resistivity substrate of commercial CMOS processed chips. The generated charge is kept in a thin epi-layer atop the low resistivity silicon bulk by potential wells that develop at the boundary and reaches an n-well collection diode by thermal diffusion.	2016 : production of CPS for the ALICE-ITS upgrade 2018/19 : production of CPS for the micro-vertex detector of the CBM experiment at FAIR/GSI 2018/19 : validation of light double-sided ladder concept combining highly granular sensors on one side with timestamping sensors on the other side < 2020 : validation of power pulsing of double-sdied ladders inside a high magnetic field 2022/23 : finalisation of the R&D on various CPS adapted to the different layers of a very high performance vertex detector at the ILC	Until 2018-2019: Development and production of CPS for the ALICE-ITS and CBM-MVD Development of various CPS optimised for the different layers of a vertex detector at the ILC, with emphasis on bunch tagging Development of low material double-sided ladders
DEPFET	University of Barcelona, Spain University of Bonn, Germany Heidelberg University, Germany Giessen University, Germany University of Göttingen KIT Karlsruhe, Germany IFJ PAN, Krakow, Poland MPI Munich MPG HLL Munich, Germany Charles University, Prague, Czech Republic IFIC, CSIC-UVEG, Valencia, Spain DESY, Hamburg, Germany IFCA, CSIC-UC, Santander, Spain	The DEPFET technology implements a single active element within the active pixel by integrating a p-MOS transistor in each pixel on the fully depleted, detector-grade bulk silicon. Additional n-implants near the transistor act as a trap for charge carriers created in the substrate (internal gate), so that they are collected beneath the transistor gate.	2014: Full-scale 75 µm thin Belle II ladder in beam test at DESY	Development of die-attach technology Full-scale test of all ASICs on ladder Integration of read-out and steering ASICs on pixel sensor using flip-chip technique and microscopic solder ball bump-bonding Production of Belle II vertex detector modules Tests of the last version of the DHP chips Engineering design for all-silicon module with petal geometry required for ILC Detailed characterization of device response Design of ancillary ASICs, taking full responsibility for future design cycles of the FE read-out chip, called Drain Current Digitizer
FPCCD	KEK Shinshu University Tohoku University JAXA, Japan Aerospace Exploration Agency	Fine Pixel CCD sensors have pixel sizes of 5 µm and a fully depleted epitaxial layer with a thickness of 15 µm	Fabrication of real size (12.3 mm × 62.4 mm) sensors with 50 µm total thickness Neutron irradiation of a small (6 mm × 6 mm) FPCCD sensor Construction of a prototype cooling system and demonstration of cooling betwe	Characterization of FPCCD sensors including beam tests and radiation damage studies Development of FPCCD sensors with a pixel size of 5 µm Construction of prototype ladders for the inner layers of a vertex detector
3D Pixels	Brown University Cornell University Fermilab Northern Illinois University SLAC University of Illinois Chicago	3D technology allows very fine pitch (4 µm) integration of sensors with multiple layers of electronics, allows interconnection oto both the top and bottom of devices, and provides techniques for low mass, thinned devices.	Completed multi-year ef 3D technology, consistin with Direct Oxide bondi TSV. Received readout wafer cessed with TSV and DB Currently working on ac	
SOI	KEK University of Tsukuba Tohoku University Osaka University	In the Silicon-On-Insulator (SOI) technology the sensing and processing functionalities are separated in different layers; the sensing is provided by a high-resistive substrate connected through an insulating layer with the processing layer.		
CLICPix	Cambridge University CERN University of Geneva Karlsruhe Institute of Technology (KIT) University of Liverpool SLAC Institute of Space Science Bucharest Spanish Network for Linear Colliders	Hybrid pixel-detector technology comprising fast, low-power and small-pitch readout. ASICs implemented in 65 nm CMOS technology (CLICpix) coupled to ultra-thin planar or active HV-CMOS sensors via low-mass interconnects.	Beam tests of prototype sors (50–300 µm) CLICpix demonstrator A Beam tests of assemblie tween CCPDv3 HV-CM ASICs Power-pulsing demonstr Prototypes of carbon-fib Full-scale thermal mocku gion	

LCTPC R&D Summary Table:

R&D Technology	Participating Institutes	Description / Concept	Milestones
Asian GEM	Saga, KEK, Hiroshima, Kindai, Kogakuin, Iwate, Nagasaki IAS, Tsinghua	Design of an endcap readout module with a stack of two thicker laser etched polymer-based GEMs and pads	2010-2013: Several test beam campaigns were perfo readout modules.
GEM	DESY, Hamburg Bonn Siegen	Design of an endcap readout module with a stack of three standard CERN GEMs and pads	2009-2013: Several test beam campaigns were perfo readout modules.
Resistive Micromegas	CEA Saclay, Carleton	Design of an endcap readout module with a Micromegas gas amplification stage, a resistive layer for charge dispersion and integrated readout. Construction of 11 modules.	2010-2015: Several test beam campaigns were perfo seven readout modules, covering the complete LP-e
GridPix ConceptGEM + pixel readout	Bonn, NIKHEF, CEA Saclay Bonn, Siegen	Design of an endcap readout module with a highly pixelized readout with GridPixes. These devices consist of a Micromegas mesh built by postprocessing technology on a pixel ASIC. Alternatively a GEM-stack is used as a gas amplification stage.	2009-2015: Several test beam campaigns with up t were performed. The three modules featured a total and this test beam was performed in March/April 20 strated that a large area could be covered with Grid 100 GridPixes per module could be operated.
Field cage	DESY	Design and construction of a TPC field cage	2009: A first prototype has been built and is used a DESY
Electronics	Lund, CERN, CEA Saclay	Design of a readout electronics fit for test beam operation at T24/1 at DESY and for investigation the requirements of the ILD-TPC electronics.	2009: Sofar, readout systems based on the AFTER chip have been used with 10,000 channels each.
DAQ	Lund, ULB-VUB, Hubei	Design of a data acquisition system fit for test beam operation at T24/1 at DESY.	Sofar, DAQ systems for both readout systems (AFT have been set up.
Endcap	Cornell	Study of different endplate designs for an ILD-TPC with CAD programs and production of smaller endplates fit for operation at test setup at T24/1 at DESY.	A detailed model of the endplate was implemented in and in 2009 a first endcap for the test beam setup ha several years ago. A new version also fulfills the req material budget and will be used from 2015 onward
	CEA Saclay, DESY	Mechanical studies for ILD-TPC regarding the effect of pressure, weight, hanging/support schemes on the mechanical deformation of the endplate and field cage.	First studies have been done.
Calibration	BNL, CERN, Indiana, Kolkata	Laser calibration system, Alignment/calibration of the TPC, Integration with other tracking systems	
Study of systematic effects	Victoria, Kolkata	Field distortions are a major source uncertainties in track reconstruction. The sources of these distortions are studied and minimized.	
Analysis software	DESY, Carleton, CEA Saclay, KEK, Saga, Siegen, Tsinghua	Development of a software package MarlinTPC, which serves all groups for reconstructing and analyzing the test beam data and for simulation, reconstruction and analysis of ILD events.	MarlinTPC is well developed and the key analysis t ses.
Ion backflow/Gating	Japanese Univers., KEK, Tsinghua, Kolkata, DESY	The ion back flow from gas amplification stages is a major source for time dependent field distortions and has to be suppressed as much as possible. With simulations and experimental setups the minimization of ion production and the reduction of the back flow by a gating device are under study. Field distortions are a major source uncertainties in track reconstruction. The sources of these distortions are studied and minimized.	Simulations have shown, that all gas amplification s many ions into the drift volume and a gating dev 2014: A first MPGD-based device, a Gating-GEM, ha and is being compared to a standard wire gate.
Cooling	KEK, Saga, NIKHEF, Saclay, Kolkata	Cooling is important to divert the heat produced by the readout electronics at the endplate. The temperature influences the gas gain and drift properties in the gas and has to be kept as stable as possible to achieve a reliable measurement.	2014: A CO_2 cooling plant has been purchased and beam site. First results show a significantly reduced t dient due to heating at the endplate.

Detector R&D Liaison Report: Summary Tables

CALICE R&D Summary Table:

R&D Technology	Participating Institutes	Description / Concept	Milestones	Future Activities
Scintillator ECAL	Nihon Dental University Shinshu University Tokyo University, ICEPP Tsukuba University			
SiliconECAL ILD	LLR / Palaiseau LAL / Orsay LPNHE / Paris University of Tokyo Kyushu University SKKU / Suwon, Korea LPSC / Grenoble OMEGA / Palaiseau	High granularity ECAL (≈ 4000 channels/dm^3). Active sensor: square matrix of about 5 × 5]mm^2 PIN diode pixels produced from one high resistivity Si wafer. 4 sensors are glued to PCB holding fully integrated read-out electronics and passive cooling. Absorber: self-supporting modular tungsten in carbon-fiber structure.	2013–: tests of several layers of technological prototype with one sensor per PCB. 2014–2015: Design, production and first tests of prototypes with 4 sensor PCBs. Sensors are glued to PCB by a robot. Design of a distributed, quality controlled assembly chain of detector elements.	2015– SPS beam tests of a new several layer prototype. Each layer has one PCB with 4 sensors (1024 pixels of 5.5 × 5.5 mm^2). Documentation of prototype production steps for future industrial mass production. Tests of sensors of various designs / manufacturers. Optimization of DAQ electronics. Design, production and tests of ILD-like detector element with several PCBs connected consecutively and readout from one end.
SiliconECAL SiD				
AHCAL	DESY Hamburg Heidelberg MPI Munich Wuppertal Mainz Omega CERN ITEP MEPHI Dubna Prague NIU Tokyo University, ICEPP Bergen Shinshu	The analog hadron calorimeter is based on small plastic scintillator tiles read out with SiPM. It uses fully integrated electronics with power pulsing, auto-trigger and time-stamping capability.	2014 - multi-layer test beam campaign at CERN with technical prototype electronics, including large-size layers (4 HBUs) 2015 - First beam tests of full HBU with SMD SiPMs fabricated with automated assembly procedure	2015 Test beams at DESY and SPS with >15 HBUs 2016/17 Test beam at SLAC with 15 layer EM stack, powerpulsing & ILC time structure, tests in magnetic field- Further develop SMD SiPM HBUs, explore "mega-tile" options Hadronic beam tests with a prototype with 1 m^3 fully instrumented volume (depends on pending funding request)
DECAL	University of Birmingham (inactive) University of Bristol (inactive) Imperial College London (inactive) Queen Mary, University of London (inactive) Rutherford Appleton Laboratory (inactive)	The digital electronic calorimeter (DECAL) proposes to use monolithic active pixel sensors (MAPS) for the read-out of the silicon-tungsten ECAL. The pixels are small enough to count the number of secondary particles of the particle shower, hence the digital calorimeter.	Four TPAC 1.2 sensors were tested at CERN (2009) and DESY (2010). The tests validated the INMAPS process and demonstrated that sensors with a high-resistivity epitaxial layer can meet the required MIP efficiency.	DECAL efforts are currently dormant. The Arachnid collaboration continues some of the work on MAPS chips.
DHCAL (RPC)	Argonne National Laboratory Boston University COE College (Iowa) University of Iowa Shanghai Jiao Tong University – SJTU (in discussion) University of Science and Technology of China – USTC (in discussion)			
SDHCAL (RPC)				
SDHCAL(micromegas)	CALICE (LAPP) CEA Saclay Institute of Nuclear and Particle Physics, Demokritos Weizman	Micromegas is a thin steel micromesh that separates the gas volume in a region of charge conversion and a region of charge multiplication. It is interesting for EM and H calorimetry because its signal is proportional to the the energy deposit in the gas. To avoid discharge upon very large energy deposits, it now incorporates resistive elements on the readout electrodes.	• Study of different resistive configurations to suppress sparking (ANR SPLAM) • Test in e-beam of 3 prototypes with integrated ASIC, show charge-up effect and spark suppression • Systematic study of a resistive configuration for spark suppression and high rate capability • Vary the RC-constant with 6 small prototypes with external electronics • Rate capability and in-beam spark study to determine the optimal RC	• Implement the best resistive configuration on an ASU (with integrated ASIC) • Build several layers, number depending on funding • If sufficient number of layers, build and operate a small calorimeter prototype equipped with resistive Micromegas and possibly also THGEM-based elements. • Full characterization in-beam of Micromegas calorimetry: response, resolution, profiles, multi-threshold compensation, MC validation.
GEM DHCAL	University of Texas, Arlington			
Thick Gems	Weizmann Institute, Rehovot Coimbra University Aveiro University	Cost-effective sampling element based on the a novel concept derived from the Thick gaseous electron multiplier	2014: 10 × 10 cm^2 discharge free (Ne/CH_4) single stage RPWELL 2015: 30 × 30 cm^2 discharge free (Ar-based gas mixture)	Early 2016: new design of 30 × 30 cm^2 detector 2016: 1 × 1 m^2 prototype 2017- testing RPWELL layer in a fully equipped (S)DHCAL
Dual Readout RD52	Texas Tech University Iowa State University INFN (Pavia, Pisa, Cagliari, Rome, Cosenza, Lecce) LIP Lisbon CERN Tufts University	Measure scintillation and Cerenkov light independently in optical fibers and measure neutron content event-by-event. Current small modules are dominated by lateral leakage.	Twenty-nine papers published in NIM on all aspects of dual readout calorimetry, including crystal dual readout. GEANT (FTFP HP) simulations of a large copper module yield an energy resolution approximately represented by $\sigma/E \approx 30\%/\sqrt{E}$ for pion-induced showers.	Measure the difference between pion-induced and proton-induced hadronic showers; measure the time history of light at 5 GHz. Build a large module 4 ton for final test of hadronic performance.

FCAL R&D Summary Table:

	oncept	Milestones	Future Activities
	SIC development)S technology, in- ata analysis	submission December 2015	Performance measurements, test-beam preparation
	me, simulations nisation	test-beam infrastructure	
	ation, connectiv- ntegration, test- ture, simulations	prototype of a thin fan-out 2016	conceptual design studies
	nd simulation		
	ition monitoring, nance studies		FPGA programming for DAQ system, semi-transparent sensor studies
	and analysis		
	production and qualification, absorber plate production and qualification	delivery of absorber plate prototypes 2016	
NCPHEP Minsk, Belarus	test-beam preparation, diamond sensor studies		
Pontificia Universidad Catolica de Chile, Santiago, Chile	FE and ADC ASIC development in 180 nm TSMC technology	prototype performance results 2017	
Tel Aviv University, Tel Aviv, Israel	sensor qualification, assembly of detector planes, data analysis and simulations	sensor plane prototype end 2015	
Tohoku University Sendai, Japan	pixel sensor in SoI technology	prototype 2017	
University of Colorado Boulder, USA	simulations		
University of California Santa Cruz, USA	radiation hardness studies for silicon and GaAs sensors		
VINCA Institute of Nuclear Science & University of Belgrade, Belgrade, Serbia	data analysis, simulations, physics performance studies		Test-beam measurements and data analysis

Detector R&D Liaison Report: Summary

- Summary of the 2014-2015 Liaison talks → Detector R&D Liaison page:
  https://www.linearcollider.org/P-D/Working-groups/Detector-R-D-liaison

- Proposal discussed within LCCDpdeb and PDAP panel this week:

  - Publication:
    Report to be available on the LCC Website
    Not to be published on arXiv or in a Journal
    Live document, updated periodically, much like online documentation

  - Authorship: 2 editors (Liaison, Deputy)
    One contact person per technology (currently 27 technologies)

- Report includes:
  R&D activities which are part of Calice, ILCTPC and FCAL and
  separate R&D efforts (e.g. vertex, dual-readout calorimetry)

  - Should not be considered as the summary to select between technologies →
    general overview of the landscape of the LC R&D activities

  - Available to general public and all newcomers interested in ILC R&D

ILC Detector Challenges: R&D Collaborations and Group Efforts

Individual R&D Efforts (e.g. vertex detectors):

- MAPS CMOS
- DEPFET
- FPCCD
- Chronopixel
- SOI
- 3D

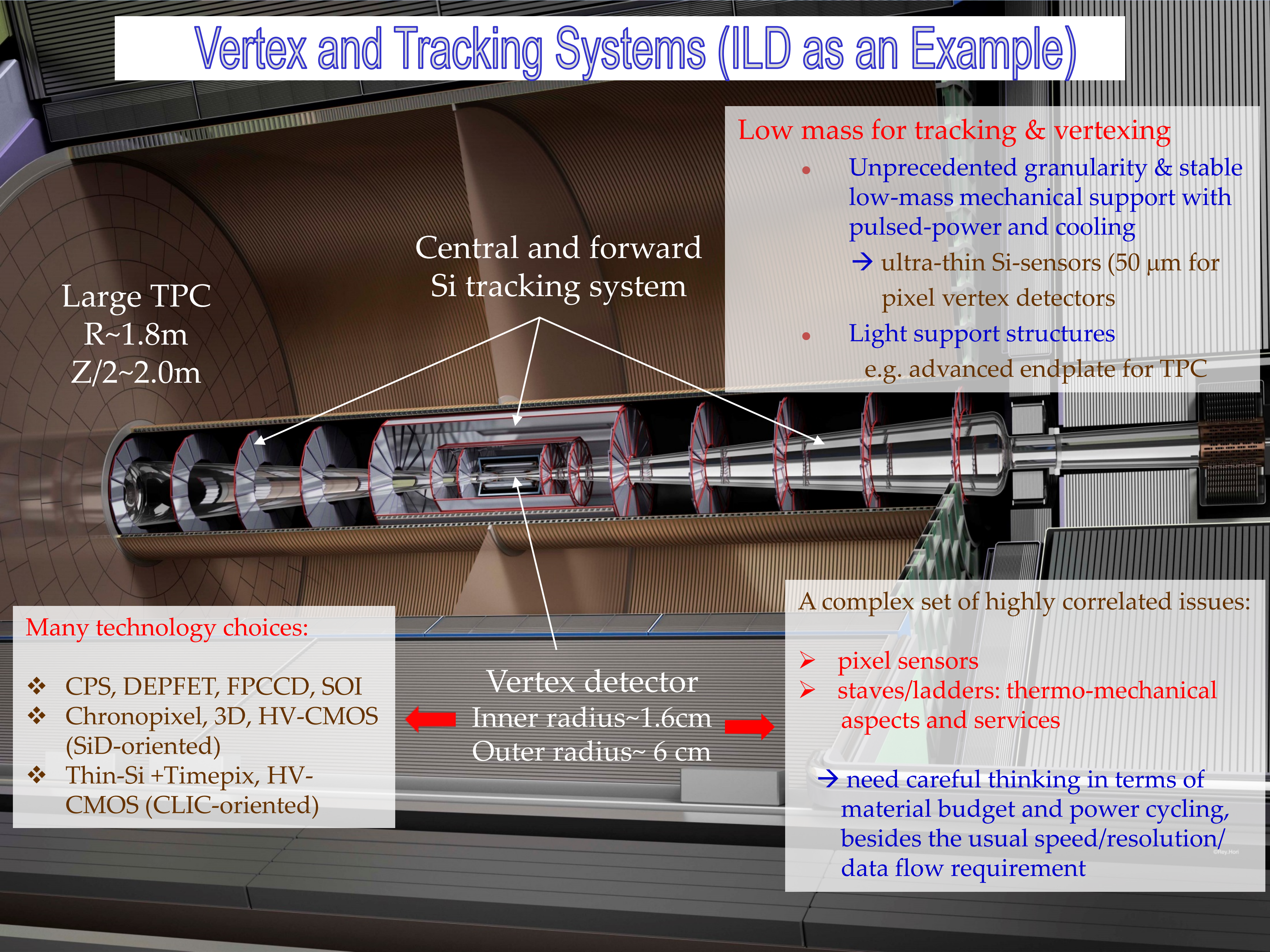
"Horizontal R&D" Collaborations:

- LCTPC: Time Projection Chamber for Linear Collider
- FCAL: Forward calorimeters for Linear Collider
- CALICE: Highly granular calorimeters for Linear Collider

❖ A lot of R&Ds is being carried out both within the ILD/SiD and through the "horizontal R&D collaborations"

❖ In the following, selection of the recent R&D results is presented → <u>special attention is given to the past/present French R&D activities</u>

Vertex and Tracking Systems (ILD as an Example)



Low mass for tracking & vertexing

- Unprecedented granularity & stable low-mass mechanical support with pulsed-power and cooling
  → ultra-thin Si-sensors (50 µm for pixel vertex detectors
- Light support structures
  e.g. advanced endplate for TPC

Many technology choices:

- ❖ CPS, DEPFET, FPCCD, SOI
- ❖ Chronopixel, 3D, HV-CMOS (SiD-oriented)
- ❖ Thin-Si +Timepix, HV-CMOS (CLIC-oriented)

A complex set of highly correlated issues:

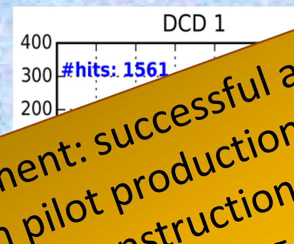
- ➢ pixel sensors
- ➢ staves/ladders: thermo-mechanical aspects and services

→ need careful thinking in terms of material budget and power cycling, besides the usual speed/resolution/ data flow requirement

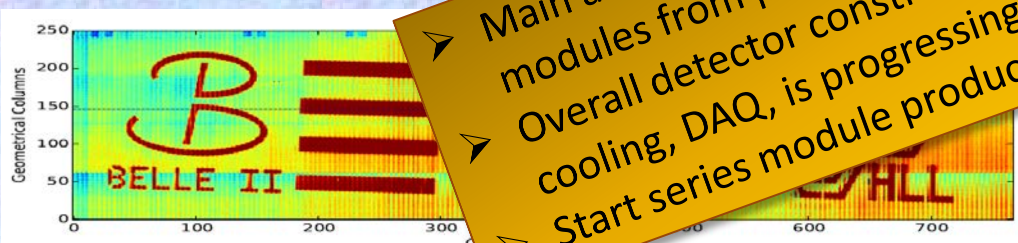
DEPFET R&D for ILC Vertex Detector

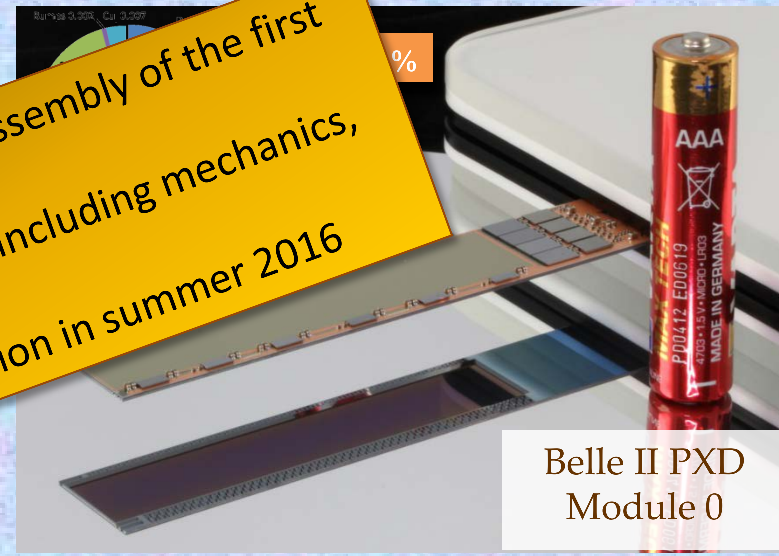
L. Andricek

- ▷ DEPFET R&D for ILC vertex detector in the frame work of Belle II PXD construction
  - ↳ Pixel sensor design and auxiliary ASICs
  - ↳ Integration to low-mass modules



- ▷ Latest achievement
  - ↳ Module 0 assembled
  - ↳ Final sensor producti

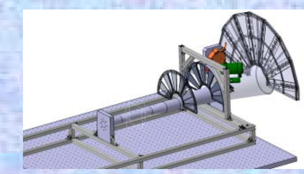


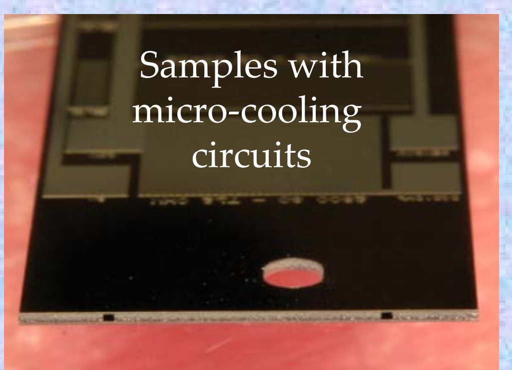


Belle II PXD Module 0

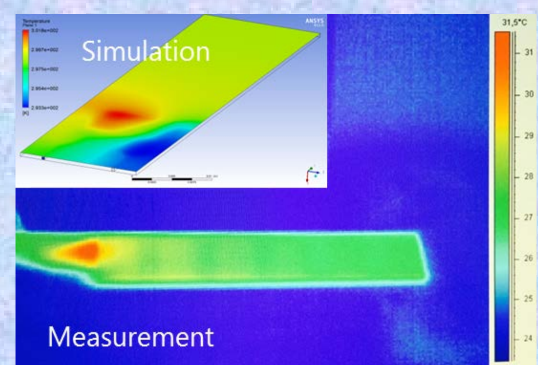
- ➤ Main achievement: successful assembly of the first modules from pilot production
- ➤ Overall detector construction including mechanics, cooling, DAQ, is progressing.
- ➤ Start series module production in summer 2016

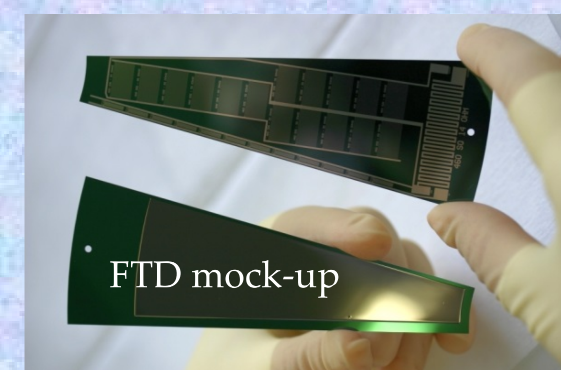
- ▷ Purely LC related activities
  - ↳ Silicon-integrated micro-cooling channels (AIDA 2020)
  - ↳ Extension of the all-silicon module concept to the vertex forward region





Samples with micro-cooling circuits





FTD mock-up

Chronopixel R&D and Status

J. Brau / N. Sinev

- Chronopixel design provides for single bunch-crossing time stamping (when signal exceeds threshold, time stamp provided by 14 bit bus)

- Prototype 1 (50x50 µm2 pixels, 180nm TSMC)

- Prototype 2 (25x25 µm2 pixels, 90nm TS…
  → Sensor capacitance larger tha…
  (because of design rule…

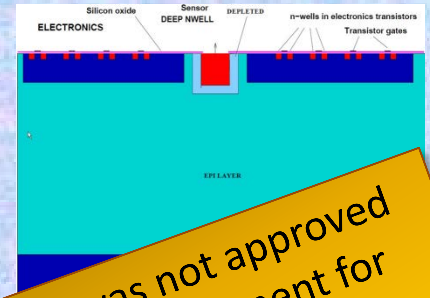
- Prototype 3 (25x25 µ…
  → Six different senso… …and
  shallow nwells and … …ns on design

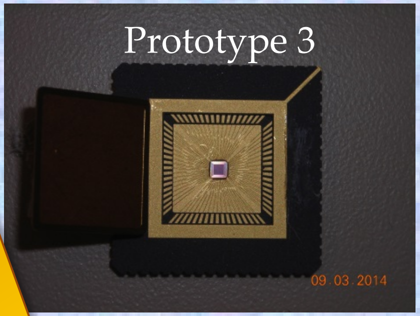
  → Main problem of large sensor capacitance due to 90 nm design rules has been solved

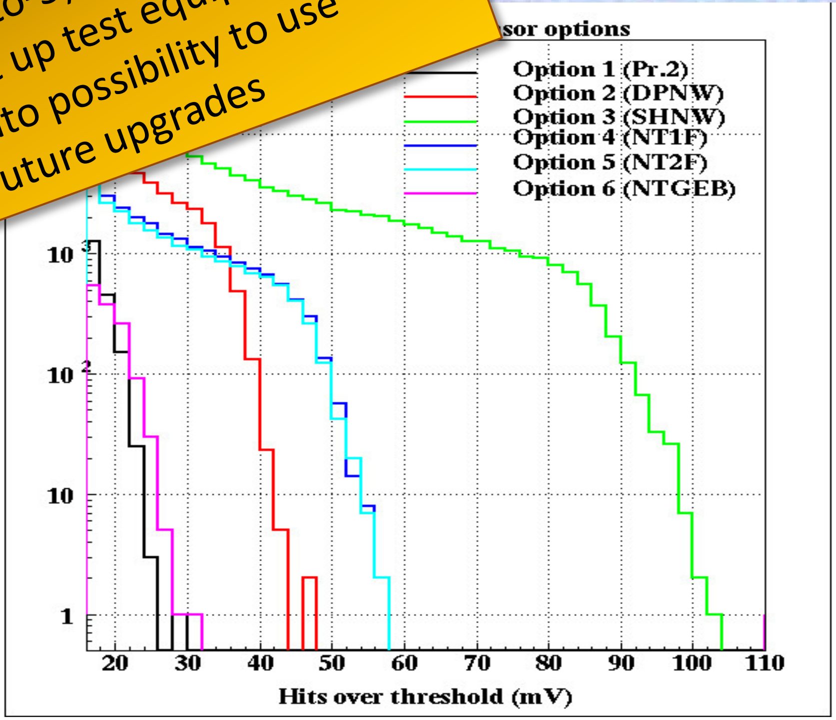
  → 4 out of the 6 options are acceptable for ILC applications (1 – 9.04 fF, 2 – 6.2 fF, 3 – 2.73 fF, 4/5 - 4.9 fF, 6 – 8.9 fF; opt. 1,6 are not accept.)

- More tests are under way to optimize the design based on minimum ionizing track efficiency.

- Future funding (beyond proto-3) was not approved
- Yale University trying to set up test equipment for proto 3 chips → looking into possibility to use Chronopixel for the LHC future upgrades







[55]Fe results for 6 sensor options:
1 – the same design as prototype 2;
2 & 3 – violate TSMC design rules – granted waiver;
4 & 5 – “natural transistors”, allowed by design rules, with gate connected to source and drain;
6 – same, as 5, but gate connected to external bias.

3D Vertical Integrated Circuits (VIP Chip)

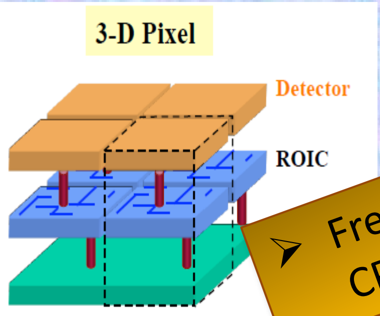
R. Lipton

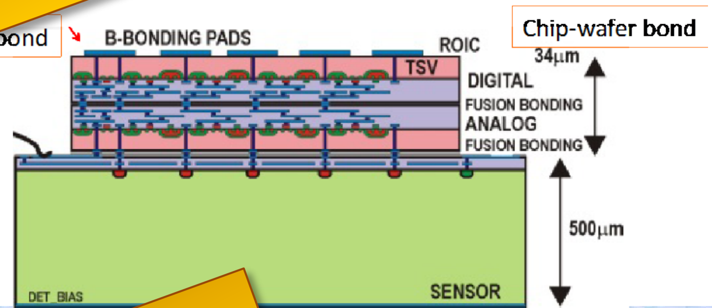
- ➢ An alternative to achieving ultra-low material budget is 3D integrated circuits:
- ❖ Fermilab 3D-IC MPW Run for HEP (2010): 3 chips VICTR(CMS),VIP(ILC),VIPIC(x-ray)

Vertical Integrated pixel (VIP) chip for ILC:

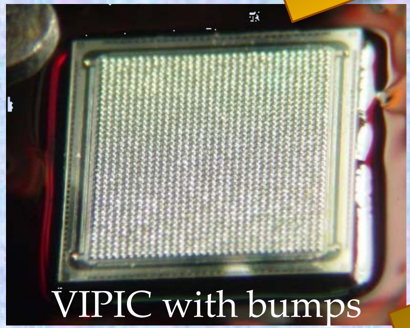
- single pixel time stamping
- 24 x 2 … els,

- Two layer 3D ASIC bonded to silicon wafer
- ASIC is thinned to TSV for metal contact to the sensor on other layer of the ASIC
- ASIC is 34 μm thick

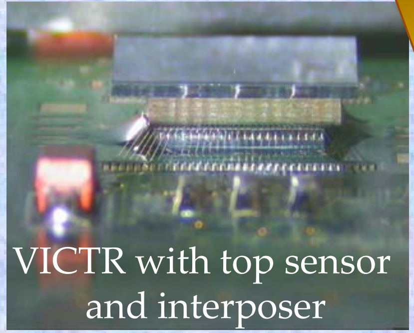




➢ French groups participated in the first run: CPPM, IPHC, IRFU, LAL, LPNHE, Grenoble

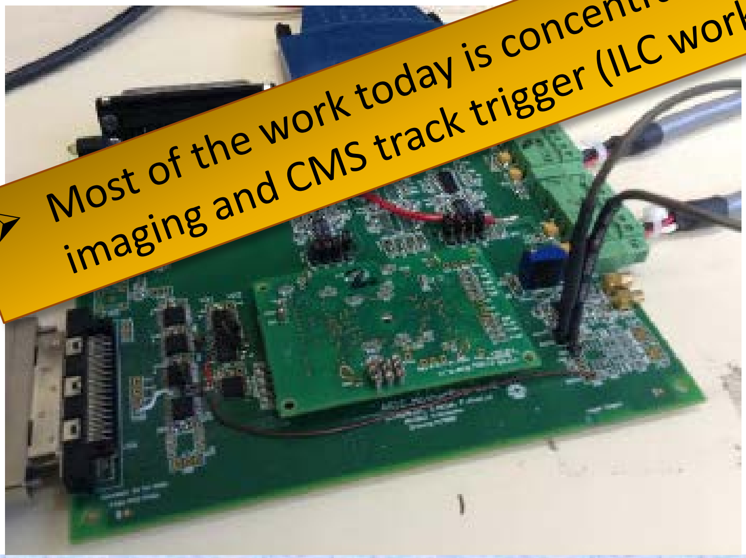


VIPIC with bumps

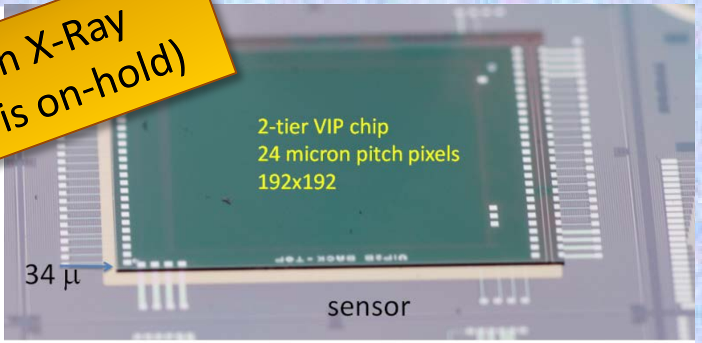


VICTR with top sensor and interposer

VIP CHIP & TESTING:



➢ Most of the work today is concentrated on X-Ray imaging and CMS track trigger (ILC work is on-hold)



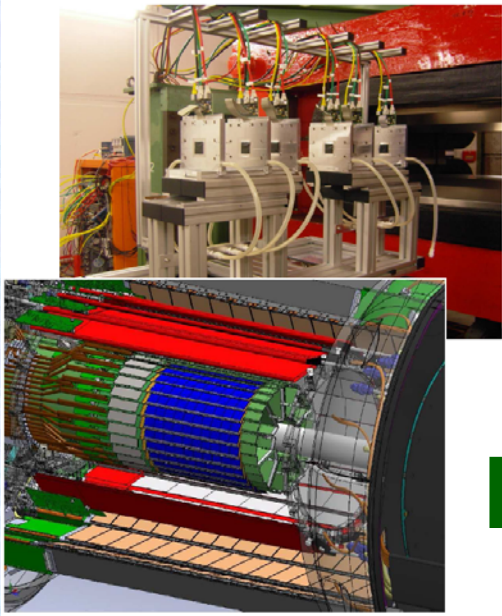
- ➢ Successfully read out all 192x192 = 36,864 pixels
- ➢ Token passes though at 189ps/pixel
- ➢ Sees source
- ➢ Issues with test pulse masking,
- ➢ odd row test pulse
- ➢ Beam test winter 2014

Monolithic Active Pixel Sensors (MAPS) – A Long-Term R&D

CMOS sensors expected to provide an attractive trade-off between granularity, material budget, radiation tolerance, speed and power dissipation

O(10^2) μs

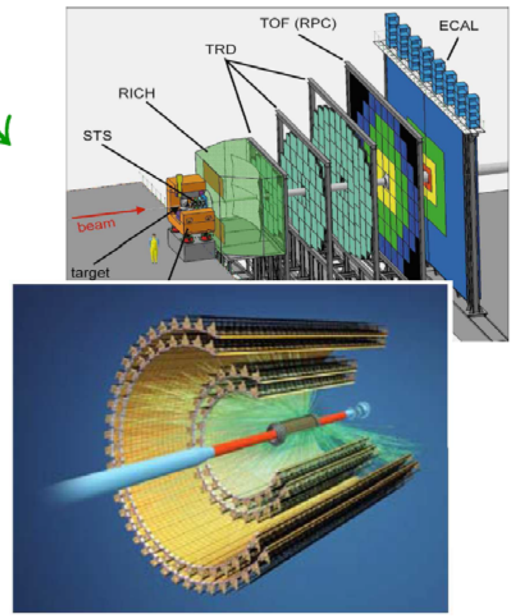
How to improve speed & radiation tolerance while preserving 3-5 μm precision & $<$ 0.1% X_0 ?



O(10) μs

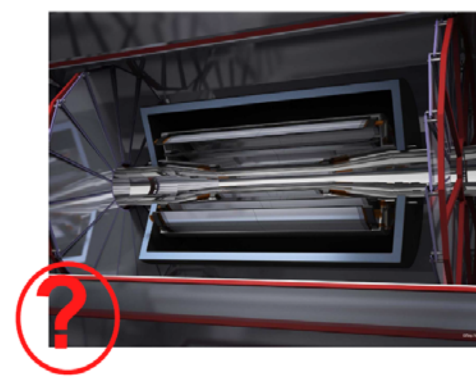
Main objective: ILC

↳ MAPS applied to <u>hadron experiments</u> with intermediate requirements



M. Winter

O(1) μs



1998-1999: IPHC introduced CMOS pixel sensors (CPS) for charged particle tracking.

EUDET/STAR	⟼	**ALICE/CBM**	⟼	**?X?/ILC**
2010/14	⟼	2015/2019	⟼	$\gtrsim$ 2020

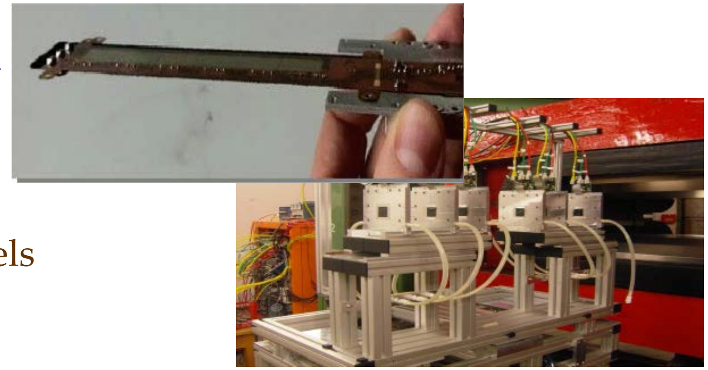
R&D on CMOS Pixel Sensors Adapted to an ILC Vertex Detector

M. Winter

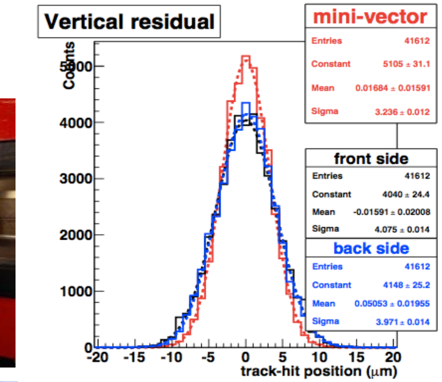
MIMOSA sensors equipping EUDET BT :

→ 0.35 µm process with high-resistivity epitaxial layer (coll. with IRFU/Saclay)

→ binary charge encoding
→ active area: 1152 columns of 576 pixels (21.2×10.6 mm2)
→ pitch: 18.4 µm 0.7 million pixels



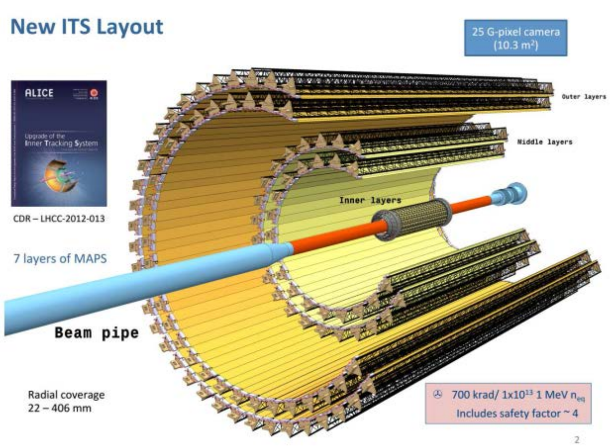
~ 3µm track resolution achieved:



STAR-PXL PHYSICS RUN OF SPRING '14

→ CPS validated for vertex detectors

→ sensor architectures developed in 0.35 µm CMOS process for ILD-VXD comply with DBD requirements



ALICE-ITS = NEW DRIVING APPLICATION OF CPS

based on a better suited (180 nm) CMOS process (TDR approved by LHCC in March '14)

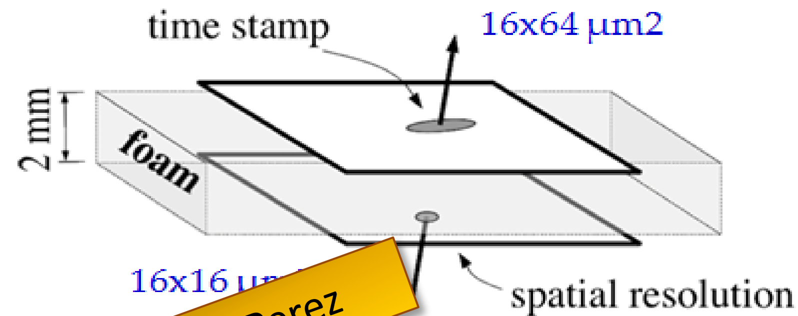
1st real scale sensor prototype adapted to 10 m^2 fabricated

→ 1st test results validate architecture in 180 nm technology
→ 2-4 times faster read-out w.r.t. 0.35 µm technology, with up to 60 % power reduction
→ Prototyping to be completed in 2016
→ New detector expected to be installed in LHC-LS2

R&D on CMOS Pixel Sensors Adapted to an ILC Vertex Detector

DOUBLE-SIDED LADDER DEVELOPMENT:

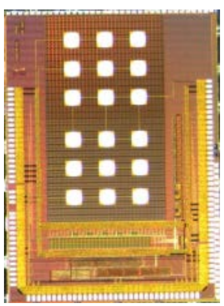
- Develop concept of 2-sided ladder using 50 µm thin CPS
- Develop concept of mini-vectors providing high spatial resolution & time stamping
- Address the issue of high precision alignment & power cycling in high magnetic field (ILC)



More details in talk of A. Perez

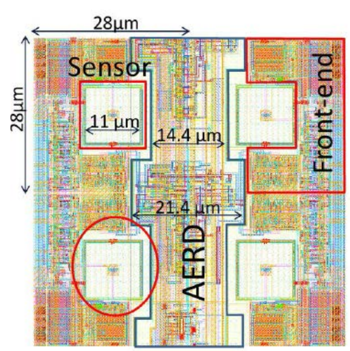
ITS Pixel Sensors: Two architectures:

Synchronous readout:



Asynchronous readout:

ALPIDE (Alice Pixel detector):

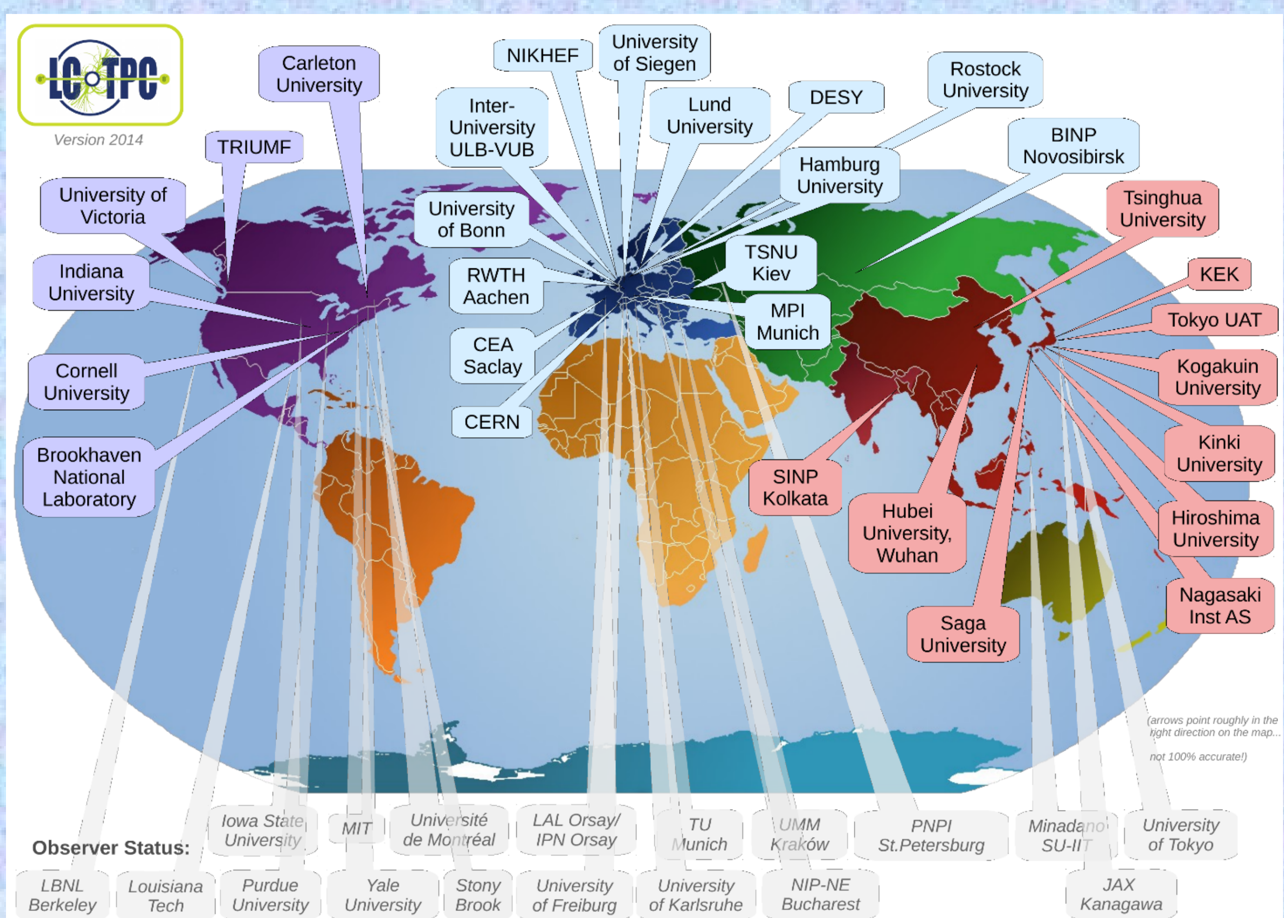


M. Winter

Main goals of the coming years are :

- improved read-out speed (single ILC bunch tagging) via new read-out architecture and enhanced sensitive volume depletion
- introduce NN in CPS to mitigate data flow from beam-related background
- realization of double-sided ladders (PLUME) equipped with two complementary types of CPS (high resolution, but rather slow and fast but less accurate); next test power cycling in mag field with impact of Lorentz forces

LCTPC Collaboration: TPC R&D



LCTPC-collaboration studies MPGD detectors for the ILD-TPC:

Europe-America-Asia:

- 30 Institutes from 13 countries
- + 18 institutes with observer status

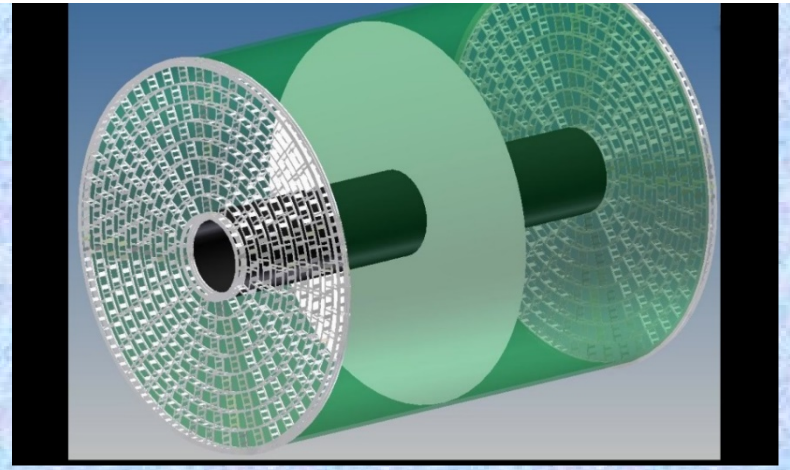
French activity encompases MicroMegas readout for ILD TPC

MPGDs in TPCs:

- Ion backflow can be reduced significantly
- Small pitch of gas amplification regions
  => strong reduction of E×B-effects

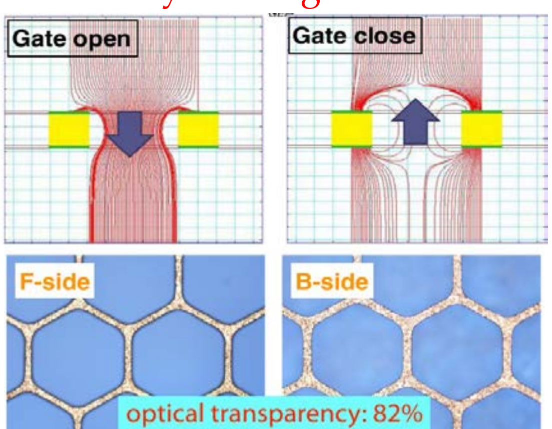
- No preference in direction
  => all 2 dim. readout geometries possible

ILC-TPC R&D: MPGD-Based readout



Primary ions create distortions in the electric field → O(10μm) track distortions

- Machine-induced bkg. and ions from gas amplification → track distortions 60 μm
  => Gating is needed
- Wire gate is an option
- Alternatively: GEM-gate



MPGDs are foreseen as TPC readout for ILC (endcap size~10 m^2):

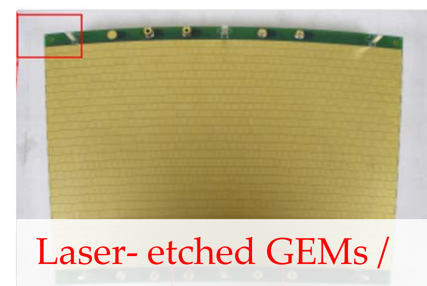
❖ Standard "pad readout" (1x 6 mm^2): 8 rows of det. modules (17×23 cm2); 240 modules per endcap

- ➢ Wet-etched triple GEMs
- ➢ Laser-etched double-GEMs 100μm thick ("Asian")
- ➢ Resistive MM with dispersive anode

➢ "Pixel readout" (55x 55μm^2): ~100-120 chips per module → 25000-30000 per endcap

- ➢ GEM + pixel readout
- ➢ InGrid (integrated Micromegas grid with pixel readout)

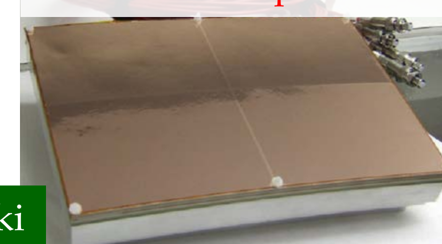
Resistive MM /



Laser- etched GEMs /

InGrid :

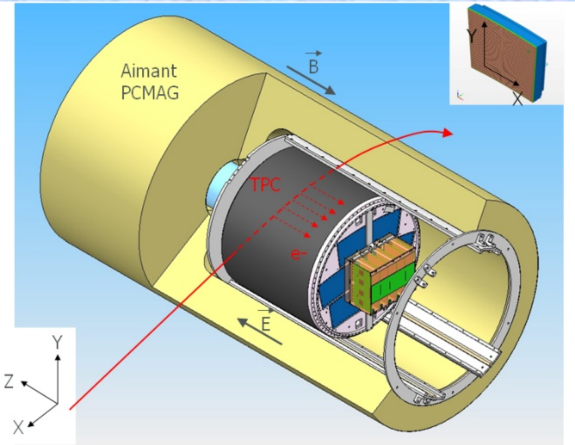
Wet-etched triple GEM:

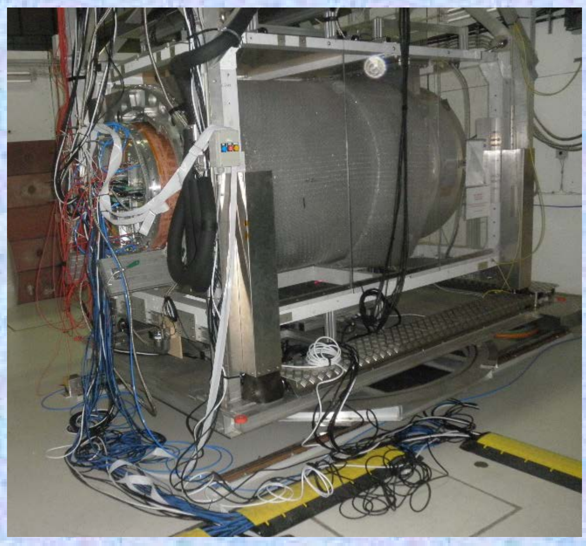


J. Kaminski

EUDET Test Facility @ DESY

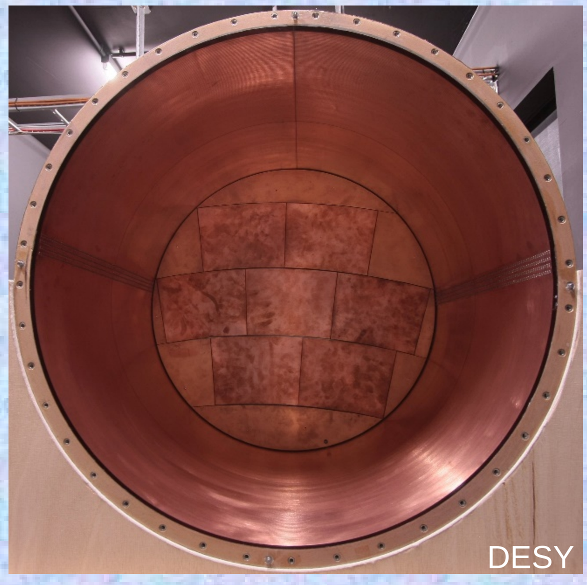
PCMAG: B < 1.2 T, bore diameter: 85 cm
Electron test beam: E = 1- 6 GeV
LP support structure
Beam and cosmic trigger





LP Field Cage Parameter:

length = 61 cm
inner diameter = 72 cm
up to 25 kV at the cathode
=> drift field: E ≈ 350 V/cm
made of composite materials:
1.24 % X_0



❖ Modular End Plate:

first end plate for the LP made
from Al: 7 module windows
→ size ≈ 22 × 17 cm^2

Large Prototype (LP) has been built to compare different detector readouts under identical conditions and to address integration issues.

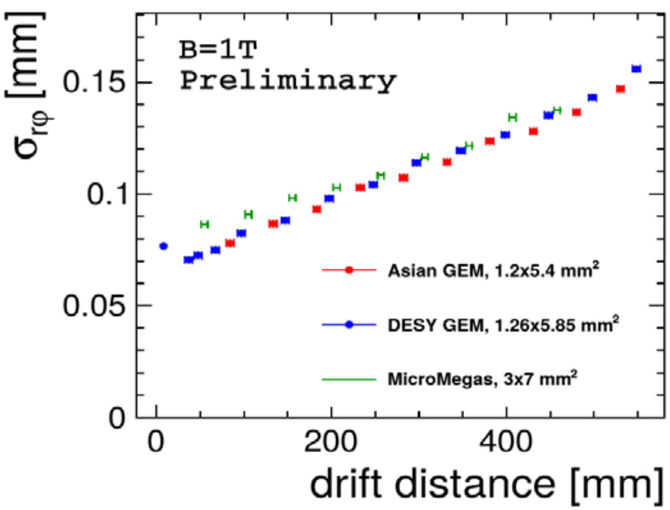
J. Kaminski

LCTPC R&D: Ongoing Activities

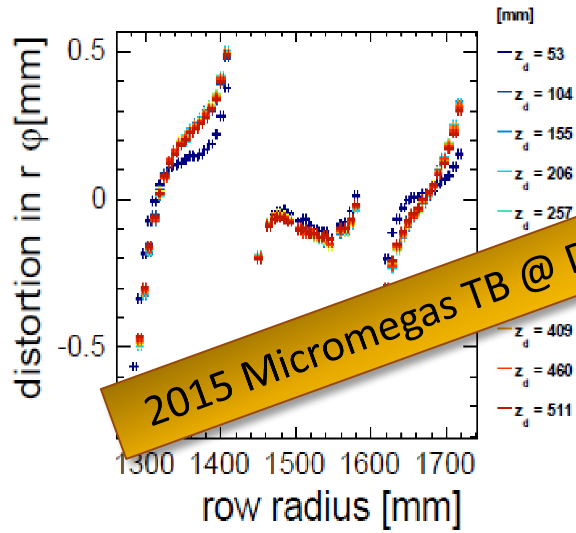
J. Kaminski

- Major effort to improve and unify the reconstruction and analysis software:
  → MarlinTPC – for example correction of inter-module field distortions.

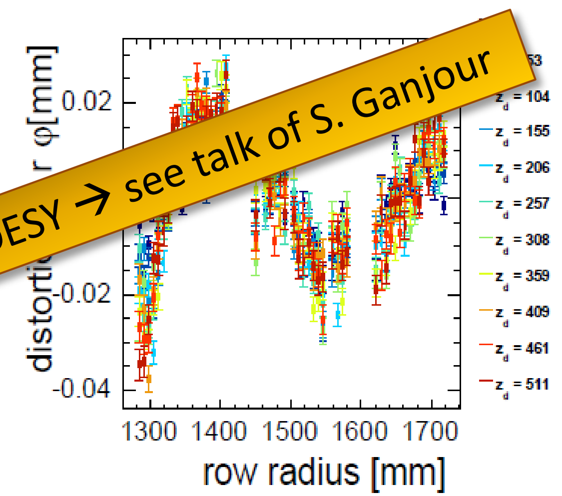
Goal for final TPC can be reached:
GEM / MM performance similar



MM: Before correction

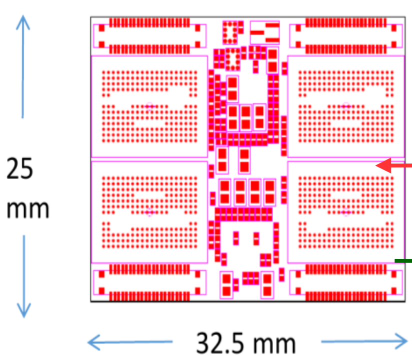


MM: After correction
(note – different scale)



2015 Micromegas TB @ DESY → see talk of S. Ganjour

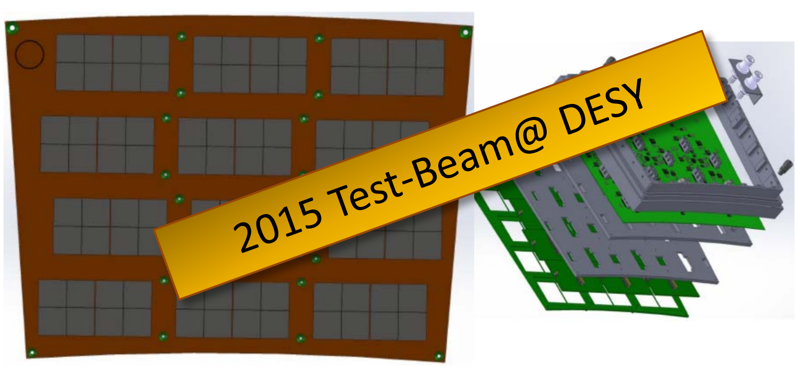
New set of electronics based on the SALTRO-16 (pad readout)



MCM board for 4 chip carriers

ASIC:

Development of the Full LCTPC module (~100 chips) @ "InGrid"s



2015 Test-Beam@ DESY

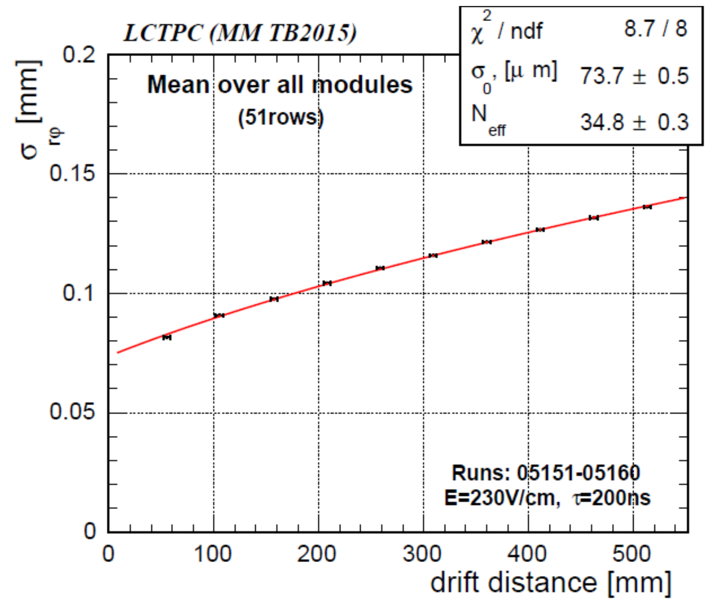
French contribution (Irfu) to LCTPC R&D: Milestones / Summary

CEA Saclay, Irfu (DAPNIA) drived the technology:

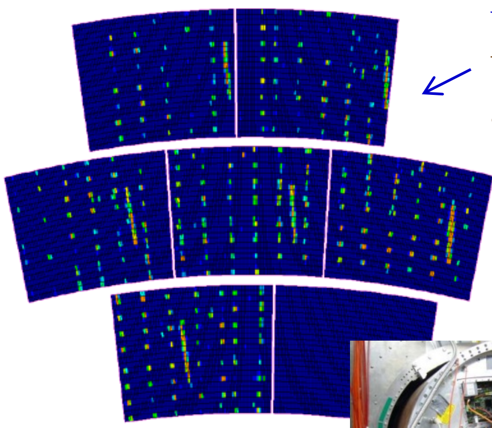
- 1992: Proposal to have a TPC by Ron Settles in 1992
- 1995: Proposal to read-out by Micromegas
- 1998-2002: Various studies with small or larger prototypes
  (drift velocities, ion backflow, gain, magnetic field)
  → DESY PRC approves the TPC R&D in 2001
- 2002-2005 : R&D with the Berkeley-Orsay-Saclay TPC
  → proof of principle. Gridpix invention.
- 2005-2007: Beam and cosmic-ray tests at KEK and DESY 5T.
  Demonstration of the resolution.
- 2008-2011: Single module tests in the DESY LP
- 2011-2015: 7 modules tests in the DESY LP
  Study of alignment and distortions.
  Integration, cooling.

P. Colas

2015 TB @ DESY: MM resolution

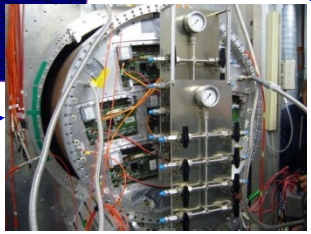


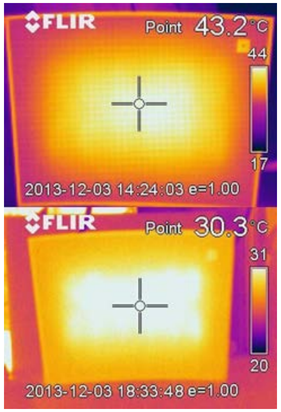
Other French labs participation:
- LAL Orsay (R. Cizeron, V. Lepeltier).
- IPN Orsay (T. Zerguerras) to data taking at KEK and to the analysis.



With beam and laser dots:
UV laser gererates MIP tracks & illuminate calibration spots

2P CO2 Cooling





- Use KEK cooling plant TRACI made in NIKHEF for CO_2 cooling
- About 30C stable temperature was achieved during operation of 7 MM modules

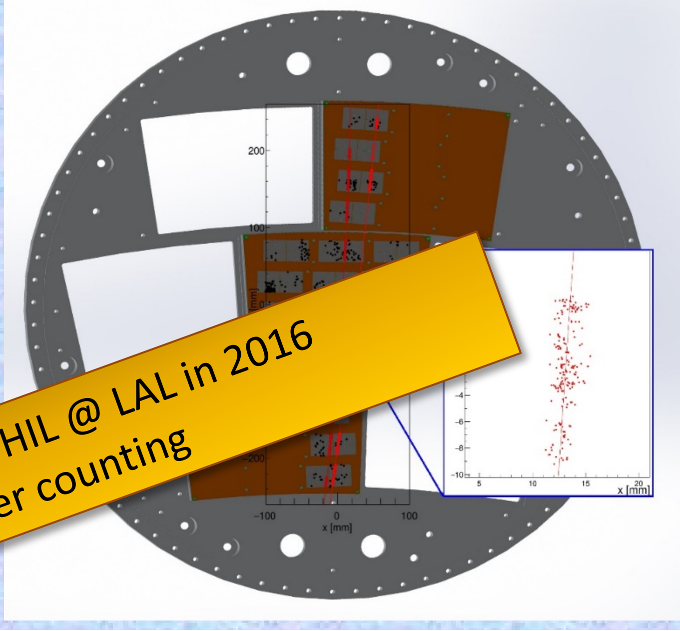
ILC Time Projection Chamber (TPC): Pixel-Based Readout

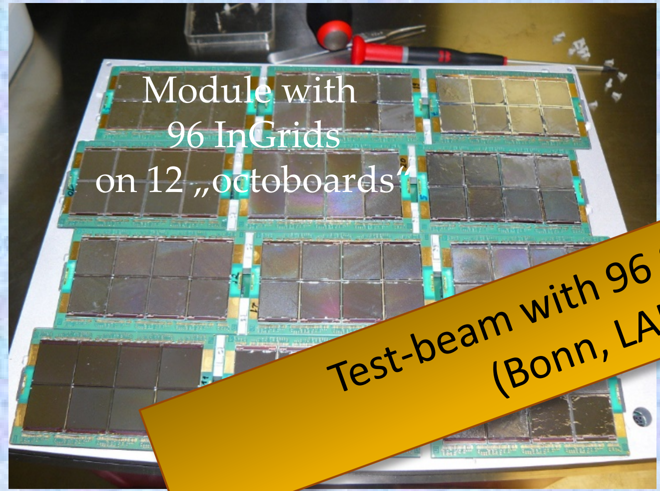
BREAKTHROUGH: feasibility shown in test-beam with 160 InGrids detectors

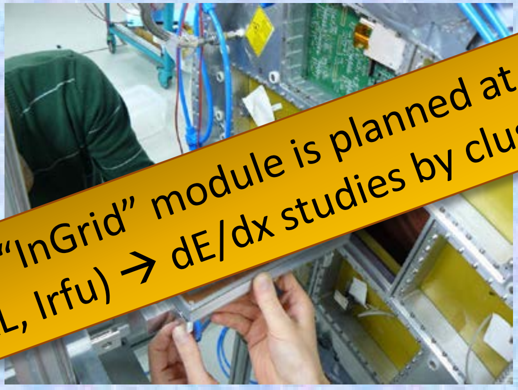
3 modules for LCTPC large prototype : 1 x 96 InGrid, 2 x 24 InGrids
320 cm² active area, 10,5 mio. channels, new readout system-
Readout 5 SRS FECs

By design:

- Single electron detection
- Time-of-arrival measurement
- High granularity; Uniform gas gain





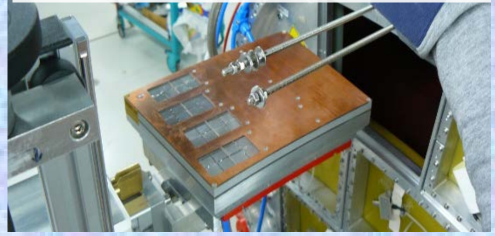


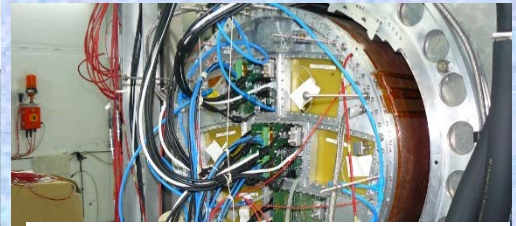
Test-beam with 96 "InGrid" module is planned at PHIL @ LAL in 2016
(Bonn, LAL, Irfu) → dE/dx studies by cluster counting

M. Lupberger

50 cm track length with about 3000 hits
→ each representing an electron from the primary ionisation.
→ demanding for track reconstruction, especially in case of curved tracks

24 InGrid installation in LP





LP endplate with 3 modules

- Physics properties of the TPC

→ field distortions; reliability
→ dE/dx resolution;delta identification
→ single point resolution
→ momentum measurement
→ Track angular effect

LCTPC Collaboration: TPC R&D Next Steps

GEM modules:

→ triple CERN GEMs: new set of modules with improved production techniques for higher GEM flatness and more reproducible module properties

→ 2 thicker GEMs: new module construction with gating grid included, decrease number of micro-discharges

J. Kaminski

Micromegas modules:

→ test different mesh sizes and different resistive materials;

→ large module with cooling and high channel density

GridPix modules:

→ Prepare GridPixes based on Timepix3 ASICs; test-beam studies

Electronics:

→ Produce a significant amount of the S-ALTRO-16 ASIC for pad-based modules

Gating grid:

→ Expected electron transparency has been demonstrated, ion absorption is to be demonstrated

Large Prototype Setup:

→ A new field cage and an external tracking telescope are under construction guaranteeing a better field homogeneity and independent knowledge of track position

Calorimeter R&D: CALICE Collaboration

GOAL:

- ❖ Development and study of finely segmented/imaging calorimeters

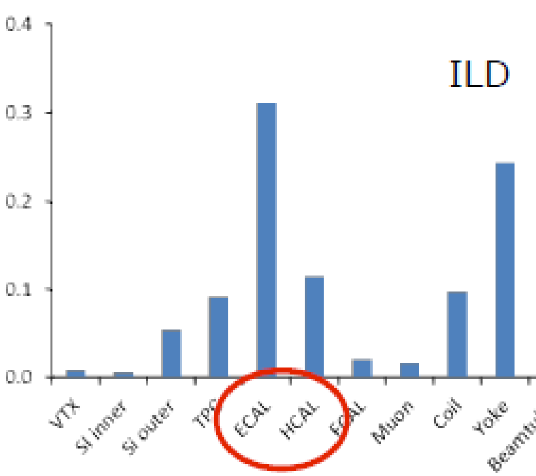
- ➢ Initially focused on the ILC
- ➢ Now widening to include the developments of all imaging calorimeter

2nd largest R&D collaboration in HEP

4 continents
19 countries
59 institutes
361 physicists/ engineers

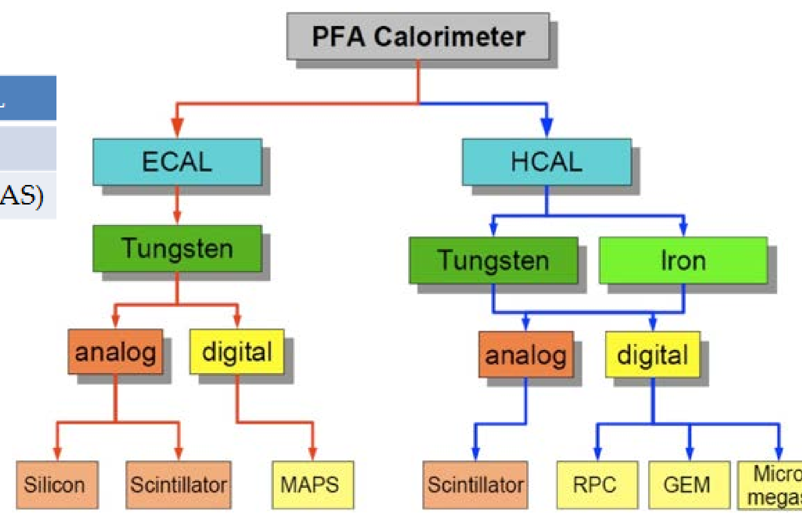
❖ R&D in Calorimetry is an LC driven effort → a marriage with "Particle Flow Algorithm" (pioneering work) has delivered a proof of principle and been established experimentally

Detector cost is driven by instrumented area rather than channel count



#ch	ECAL	HCAL
ILC (ILD)	100M	10M
LHC	76K(CMS)	10K(ATLAS)

ILD/SiD Calorimeter Concepts:



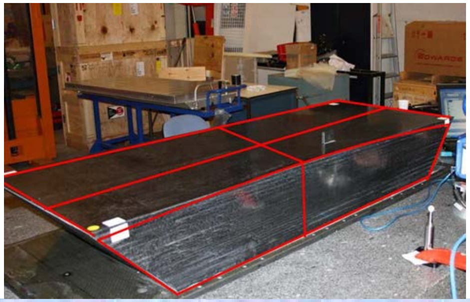
CALICE R&D: Technological Prototypes

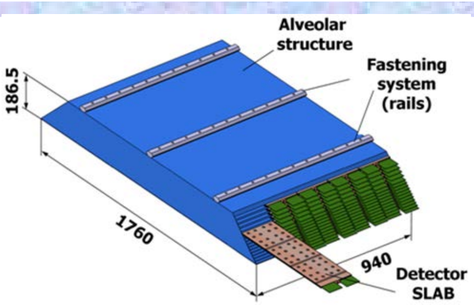
J. Repond

- ❖ 1st generation of large prototypes built/tested (SiW ECAL, Sc-W ECAl, Sc-Fe/HCAL,RPC-Fe/W HCAL (mostly without embedded electronics, integrated HV / LV, power pulsing)
- ❖ 2nd generation prototypes meant to address all remaining technical issues (scalable to the size needed for a 4π detector; not necessarily fully instrumented (at this point))

Silicon – Tungsten ECAL

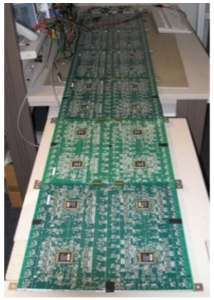
- 5 x 5 mm^2 pads
- New generation readout (embedded, power pulsing)
- Semi-automated assembly, wedge shaped mechanical structure





Scintillator – Tungsten ECAL

- Scintillator strips with MCCPs (5 x 45 mm^2)
- Application of Split Strip Algorithm → 5 x 5 mm^2 eff. Gran.
- Wedge shaped, same absorber as for SiW
- New generation readout (embedded, power-pulsing



RPC –Fe/W (1st proto with power-pulsing, self-supporting str., compact)

MPGD (GEM, THEGM, Micromegas)- Fe/W

Scintillator – Fe/W HCAL

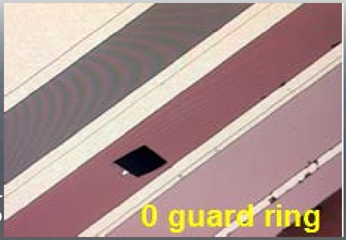
- 3 x 3 cm^2 scintillator pads
- New generation readout (embedded, power pulsing
- Wedge shaped

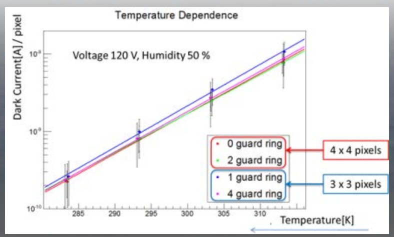
CALICE R&D: Further R&D on Active Elements

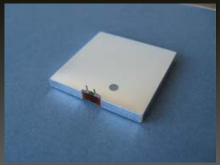
J. Repond

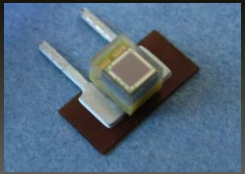
Silicon sensors

Guard ring design studies
→ segmented or no guard ring









Scintillator pads / strips

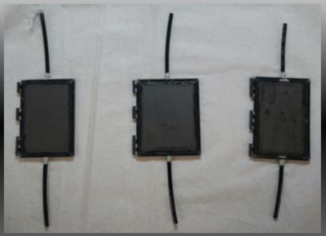
- Tiles with dimples → easier assembly, uniformity
- Wedged tip of strips → more uniform response

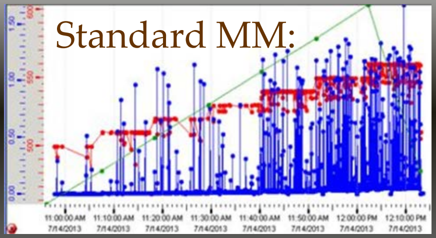
MPPC developments

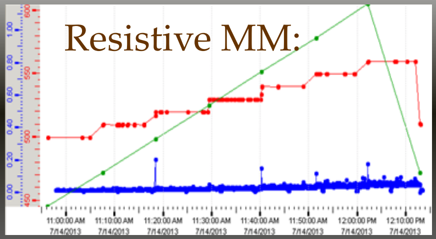
- Improved linearity, Si-purity; increased # of pixels
- Implement. of barrier (noise rate), trench (cross-talk)

Resistive Plate Chambers (RPCs)

1-glass design → beam tests (successful!)
Development of semi-conductive glass → higher rates

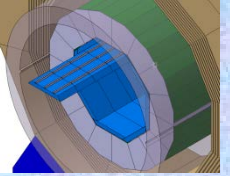






GEM / Thick GEMs / Micromegas

MM: implementation of resistive layer
→ reduced spark rate



Silicon-Tungsten (SiW) ILD ECAL

Kyushu, Tokyo Uni., LLR, LAL, LPNHE, LPSC

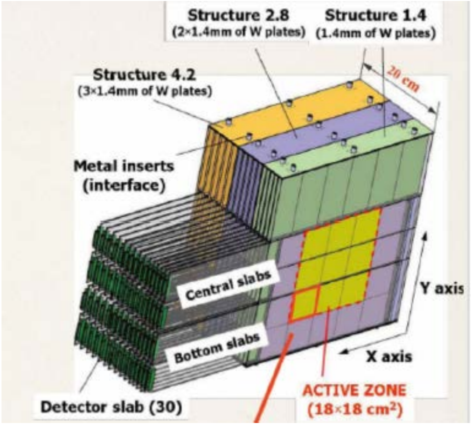
SiW ECAL: Low systematics → Perfect linearity, simple calibration, stable in time, robust
Cost reduction → 10% of bad pixels is affordable (not tracker device)

1st Physical Prototype (2005-2011):

Conceptual proof of PFA, verification of MC

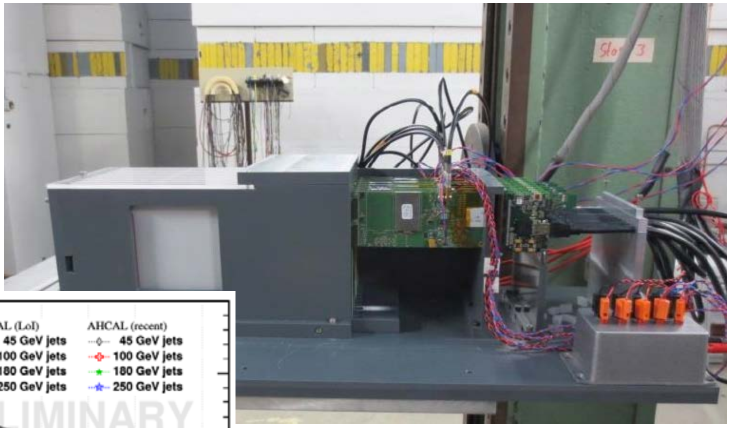
10x10 mm2, 30 layers
Electronics outside

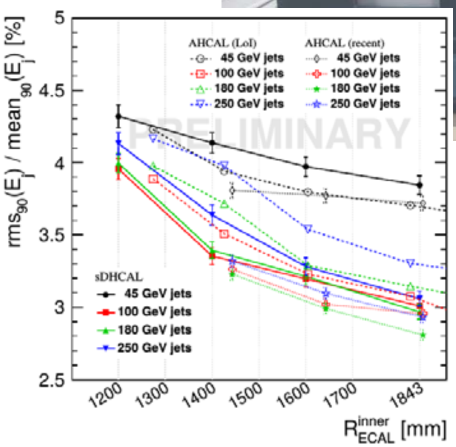
$\sigma E/E = 16.6\%/\sqrt{E} \oplus 1.1\%$,
linearity within 1%.



2nd Technological Prototype (2012-present)

- Embedded electronics
- Choice and finalize design
- Prepare mass production





Optimize performance vs cost as a function of ILD dimensions,

BROADENING THE SCOPE:

Recent interest to SiW(Pb) technology for :

- CMS endcap Phase 2 upgrade (HGCAL)
- Future circular colliders (TLEP, CEPC).

LLR: Silicon-Tungsten (SiW) ILD ECAL

J.-C. Brient

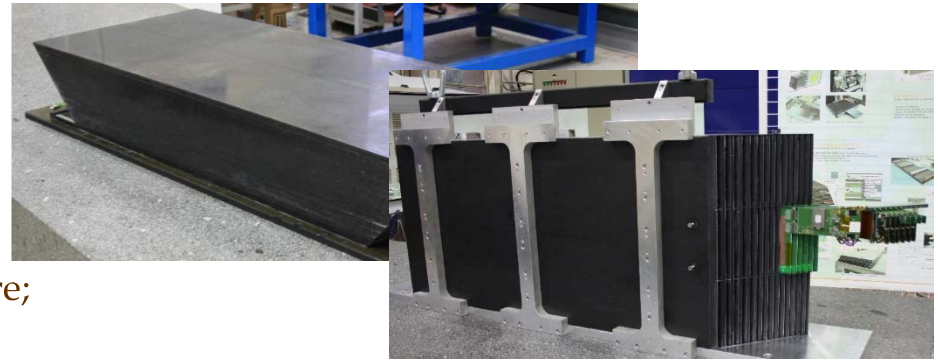
Prototype with all the key techniques needed for a large ILC detector :
Sensors, Readout, Thermal & Mechanical constraints with industrial feasibility
(2600m² of sensors, 26 MCh, 25k detection units, 3500 cassettes, 40+16 modules)

2012: Carbon-Fibre–Tungsten Mechanical prototype: 60% model of barrel module:

→ 3/5 x ILD barrel module (600 kg, 5 years R&D)
Self-standing, minimal dead zone structure for Casette hosting

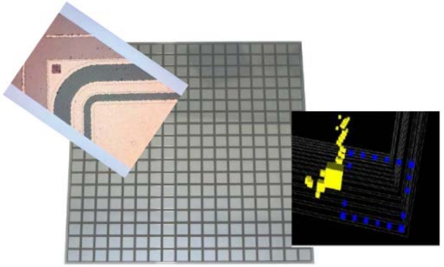
→ Mechanical simulation of large composite structure;

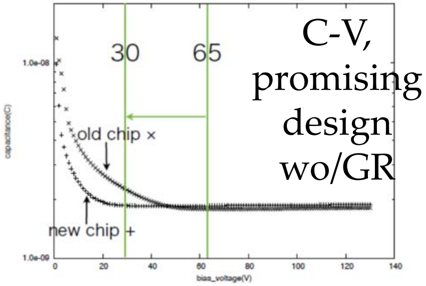
Unique object at the size of ILD detector



From 2005: Silicon sensors

- ❖ Highly Resistive Si-pin diode: Guard Rings design
- ❖ Industrial contact for production and characterisation for cost/perf optimisation
  R&D in Hamamatsu HPK (CNRS, Kyushu)
  →2.5 EUR/cm2; know-how design :"no guard ring"
  LFoundry (Europe) with CNRS
  →Larger (8') and thicker (700 um) sensors.





- ❖ Highly integrated cassette design with minimal thickness (for reduced R_M):
  - Production of a long cassette with cooling capacity (with LPSC Grenoble)

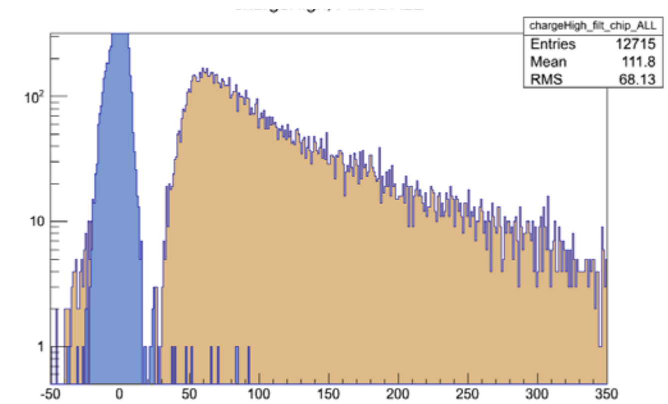
LLR: Silicon-Tungsten (SiW) ILD ECAL

J.-C. Brient

– **2010: Front-End Integration of Omega's SKIROC2 chips in Power-Pulsing & auto-trigger :**

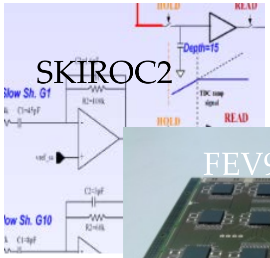
- Large dynamic .. From ¼ MIP to few 1000 mips (ILC)
- The detector units handling 1024 channels: **S/N(mip) ~15 –17 obtained** (but for a restricted dynamic)
- Long chain of detector units (8–10) for cassettes to be establishec

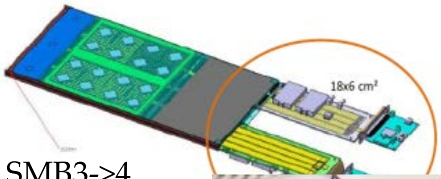
Mandatory for 100M channels device



Since 2008: Flexible DAQ for readout of 10000+ channels prototypes:

- Online monitoring: readout chip local storage ⇒ dynamic noise handling and zero suppr.
- Single cable digital DAQ
- PYRAME / CALICOES generic python low-level development





SMB3->4

Since 2005: Linear Collider Software:

– Parametrised Geometry Overlayer of GEANT4 (Mokka)
– Advanced Reconstruction Algorithms for Highly Granular Calorimeters (GARLIC, ARBOR)

⇒ Optimisation for the ECAL

LPNHE: Calice Active Sensors Unit Assembly

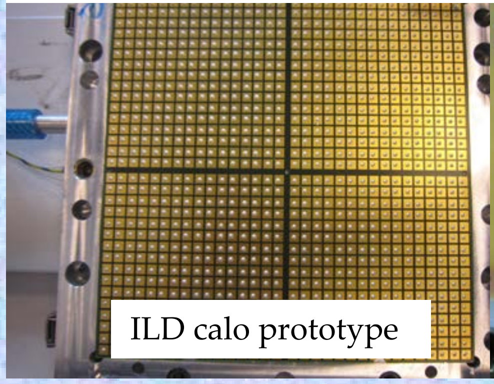
- Assembly done with gluing and positioning robots: automated system developed in the framework of the Calice R&D program for ILD SiW EM calorimeter and for ATLAS high granularity timing detector

- Electrical test to control the sensors before gluing, to check the short cuts immediately after gluing to measure the I(V) curves
- Metrology using a coordinate measuring machine (tri-dim machine): squaring, parallel edges, size, thickness flatness

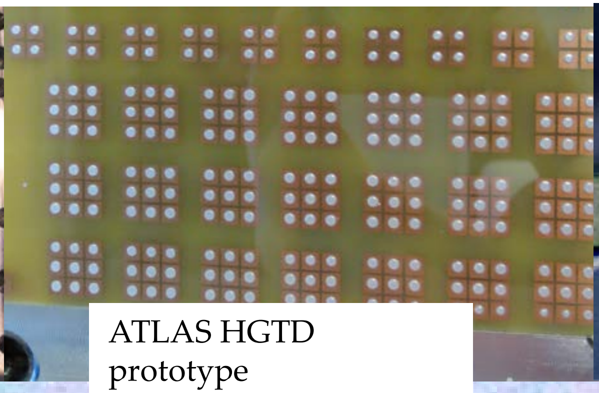
- Gluing test with glass plates

Gluing and positioning robots

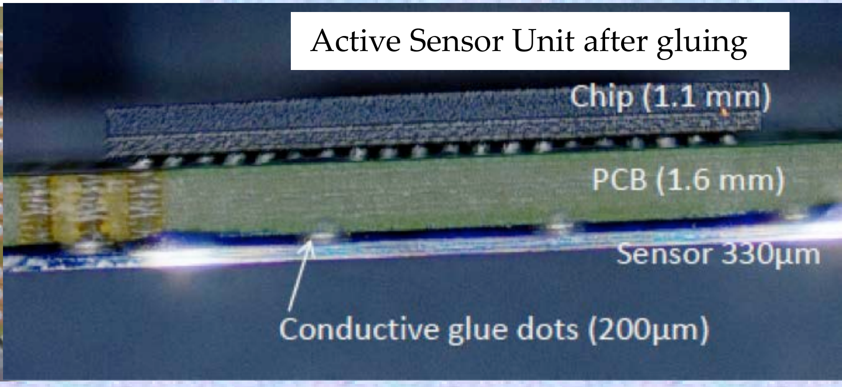
D. Lacour



ILD calo prototype



ATLAS HGTD prototype



Active Sensor Unit after gluing

- 7 layers assembled for 2015 test beam ILD prototype – 5 layers will be done in 2016
- ATLAS R&D in progress – 4 layers prototype to be built in 2016 and beam tested
- Glue radiation hardness/thermal effects to be tested
- Industrialization of the process – contacts with Eolane company

LPNHE in the ILC since the beginning:
(Jean-Eudes Augustin, François Lediberder)

- Until 2010 : collaboration SiLC (A.Savoy-Navarro)
- Since 2011 : Calice, EM Si-W (D. Lacour) – Official CALICE member > 2012

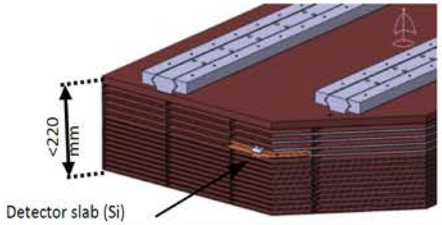
LPSC Grenoble: Calice SiW Summary (2005-2016)

Jean-Yves Hostachy

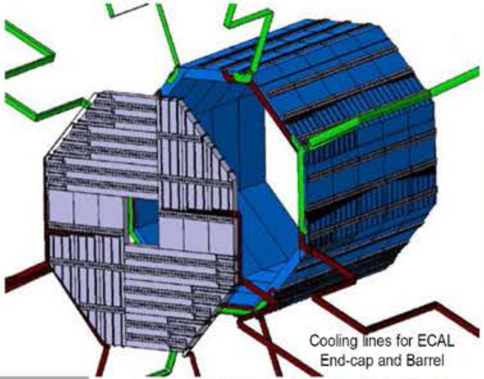
1 / ECAL End-Cap alveolar structures (CFRP + W)

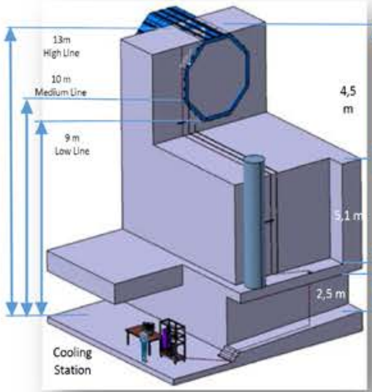

2,5 m Long End-Cap layer

1 of the 3 « standard » modules of each quarter



2 / ECAL General Cooling Integration - Leakless system - 2016

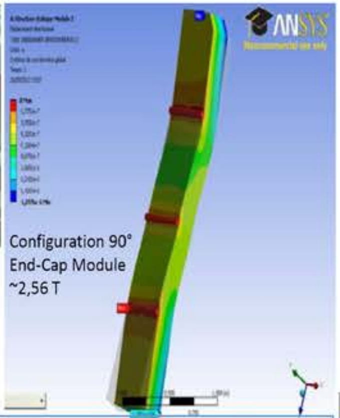

Cooling lines for ECAL End-cap and Barrel



LPSC cooling test area with a drop of 13 m

3 / Assembly and positioning of modules


Double row sized rail on Module' back

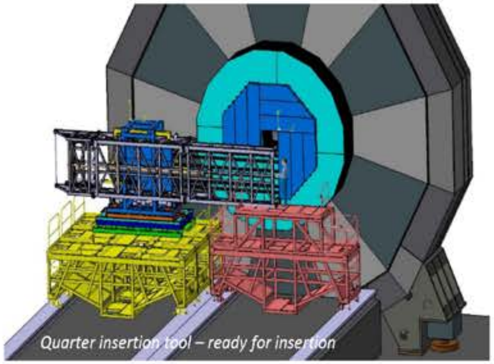


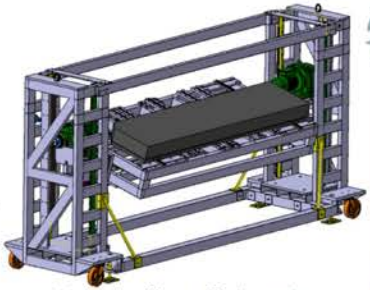
FEA Simulations / structures behaviour


Cooling station on going

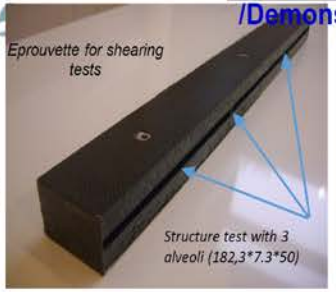

Cooling station circuitry / 2016

4 / ECAL End-Cap Integration


Quarter insertion tool – ready for insertion


Module handling tool for integration

5 / Components for prototypes EUDET Module / AIDA /Demons




End-Cap thick composite plate 13mm+ inserts for double row rails


Cooling tests on EUDET-2016

LAL Orsay: Assembly of SiW ECAL Layers

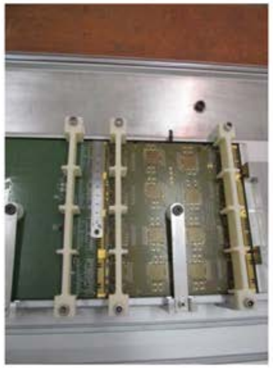
R. Poeschl

- 2003 - 2005 FLC_PHY3 ASIC, FLC_SiPM ASIC (OMEGA)
- 2005 – 2011 Beam tests with SiW Ecal physics prototype
- Since 2006 HARDROC, SPIROC, SKIROC, MICROROC (Pole OMEGA)
- 2010 Production run of ROC ASICs
- Since 2007 Study of assembly of SiW Ecal
- 2009: First thermal demonstrator (with LLR and LPSC)
- 2012: Assembly of SiW Ecal (simplified layers) technological prototypes
- 2012 – 2013:Beam tests with simplified layers (1 paper)
- 2015: Chip-on-Board PCB for SiW Ecal (With OMEGA)
- 2016: Assembly of fully equipped short layers of SiW Ecal

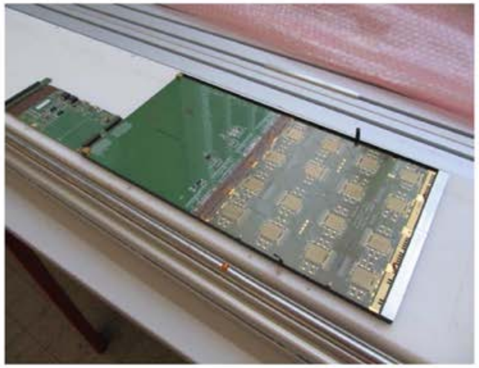
Assembly bench in LAL Workshop

Pick and place

Precise alignment



Ready for test



Assembly steps are validated with short layers

LAL assembly bench will also serve as starting point for ATLAS HGTD studies (D. Zerwas)

also synergy with HGCAL CMS (?)

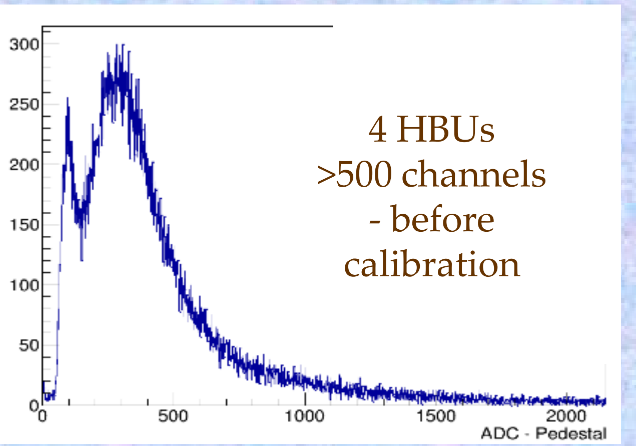
Need big step towards long layer to assure high quality product

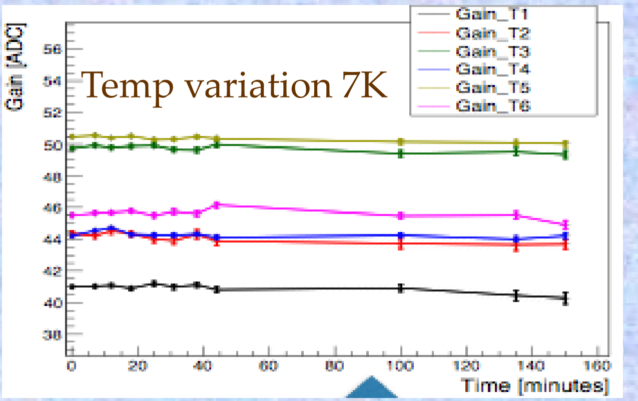
- Automated pick-and-place and alignment
- Interplay of many different working steps:
  a) Properly Assembly
  b) Continuous control of up to 8 ASUs during assembly

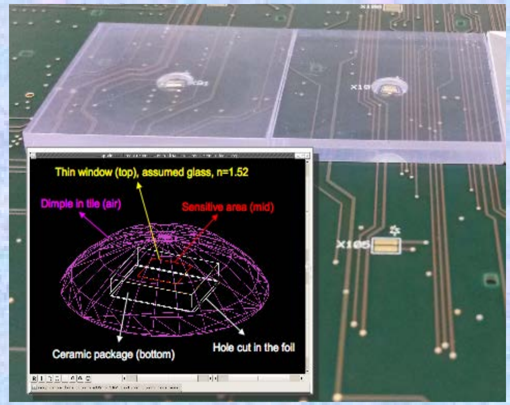
AHCAL R&D: The Scintillator Analogue HCAL

F. Sefkow

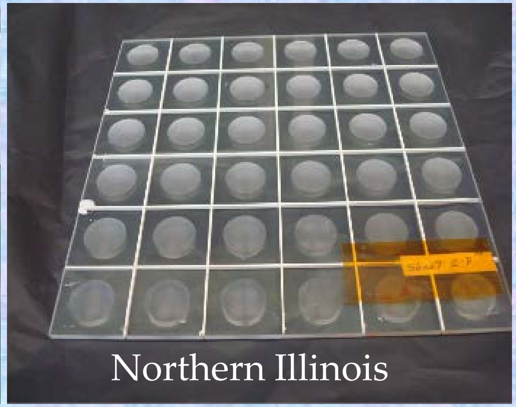
- **SiPM trends:** driven by industry, medical applications: benefits in present prototype
  - uniformity → simplification: no need anymore for light yield, gain and threshold equalisation
  - lower noise → higher over-voltage → better T stability
- **Scintillator trends:** optical coupling concepts amenable to mass production - under test in present prototype
  - No WLS fibre (blue-sensitive sensors), SiPM on board, mega-tiles



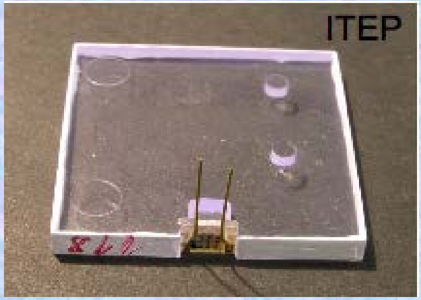




Mainz, with DESY und Uni HH



Hamamatsu sensors, on or in PCB surface



CPTA, KETEK or Hamamatsu sensors no WLS fibre

individually wrapped; KETEK sensors

AHCAL R&D: The Scintillator Analogue HCAL

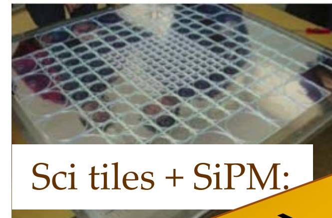
F. Sefkow

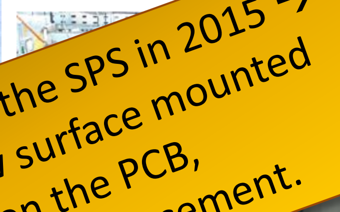
Flexible Test-Beam Roadmap towards 2nd generation prototype (synergy with ScECAL):

- General approach: proceed with system integration whilst remaining open on sensor technology side
  → possible thanks to versatile electronics

- 2014 - 2015 → 3 ECAL + 24 HCAL units = shower start finder + 4 big layers (~ 4000 channels); Fe and W absorb

Large Scale Prototypes:

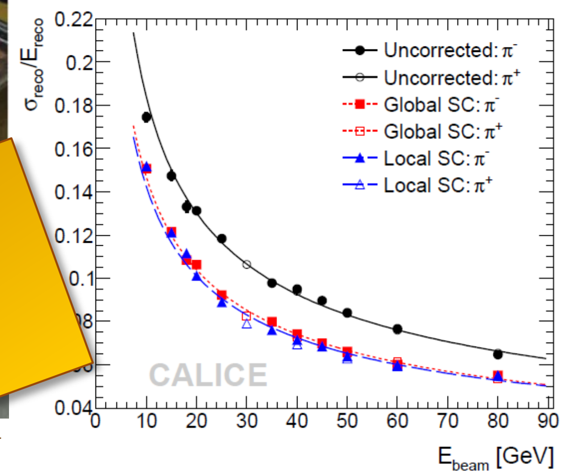




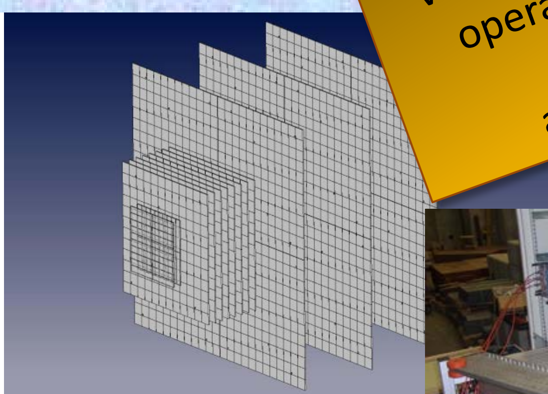
steel or W

Earlier AHCAL test-beam:

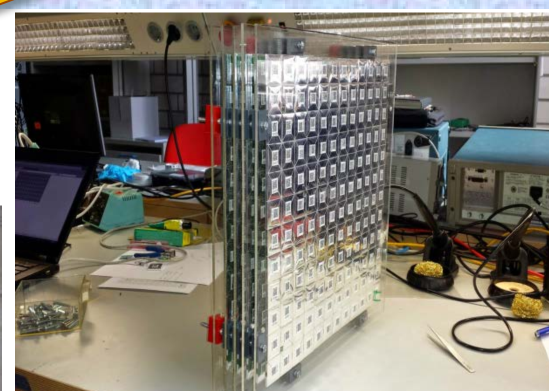
Excellent hadronic energy resolution by software compensation



Very successful test beam run at the SPS in 2015 → operation of a layer in the new surface mounted design with the SiPM on the PCB, assembled with automated tile placement.



at CERN
S in Oct and
Nov/Dec 2014

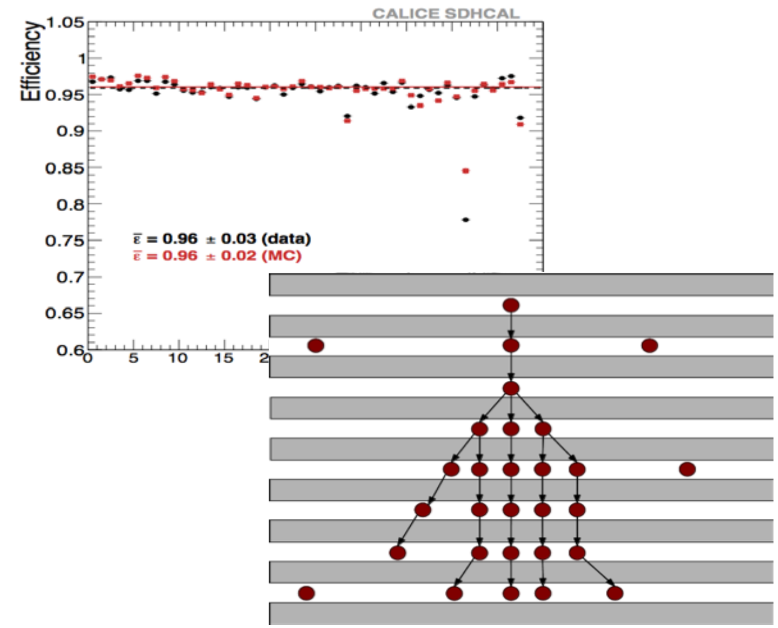


IPNL Lyon: RPC R&D for SDHCAL

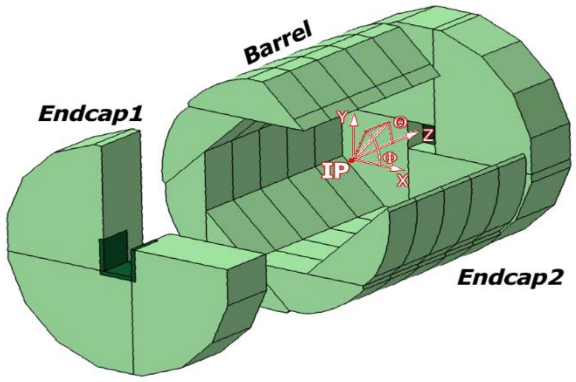
I. Laktineh

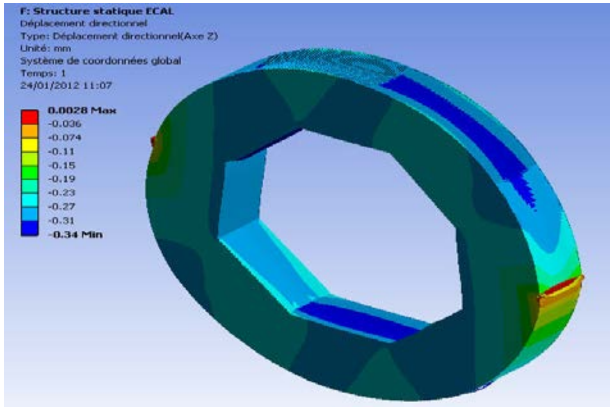
2006 :SDHCAL using GRPC is proposed
2006-2007: Development of small GRPC & HARDOC ASIC
2008: Build a technological prototype: compactness, embedded electronics and power-pulsing, self-supporting mechanical structure
2011 : The technological SDHCAL prototype is completed and commissioning achieved
2012: Beam tests at CERN (2 campaigns of 2 weeks)
2012-2014: Test-beams, data analyses, PFA simulation tools for SDHCAL
2014-2016: New campaigns of beam tests: gain correction, threshold, temperature/pressure correction.
Module0 design and production including : large GRPC, 3rd generation of ASICs, large ASUs, self-supporting mechanical structure using electron beam welding
Combined beam test with SiW

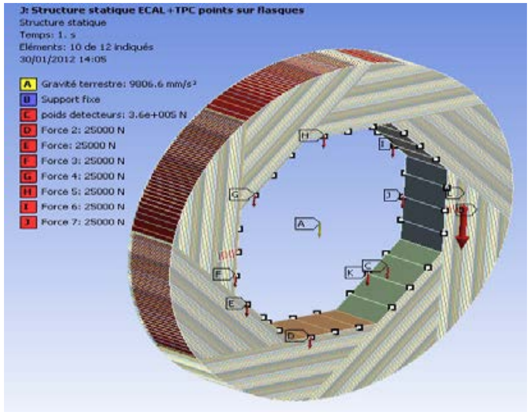
SDHCAL beam tests data analysis
SDHCAL simulation, and PFA algorithms:



SDHCAL mechanical concept, services, integration, simulation, optimization/performance studies.



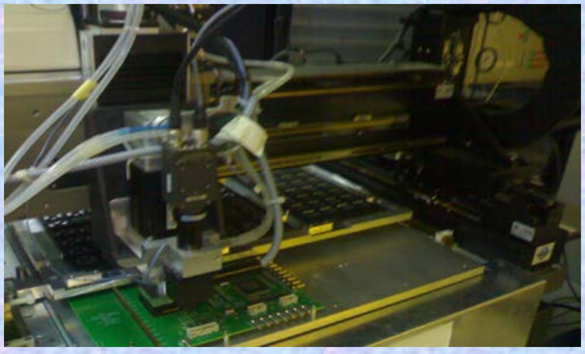


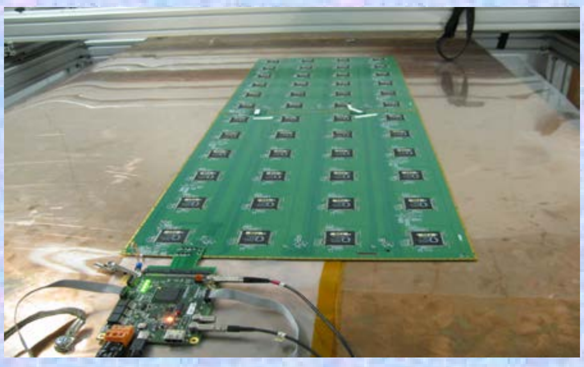


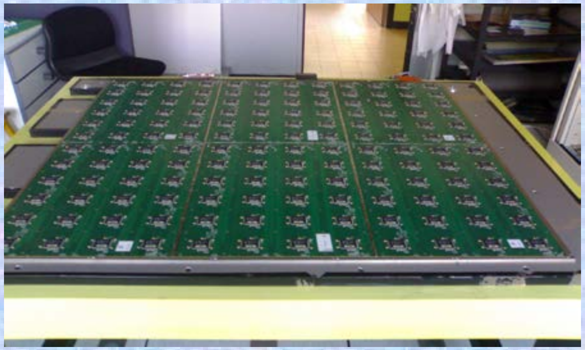
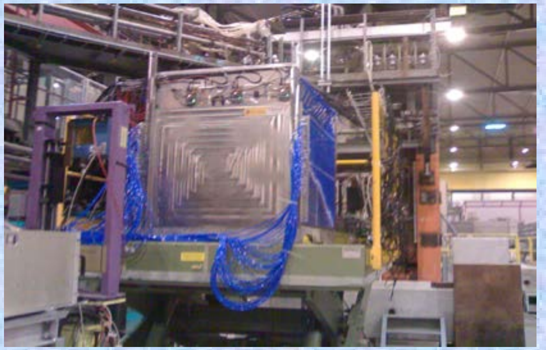
IPNL Lyon: RPC R&D for SDHCAL

I. Laktineh

Concep,construction and commissioning of the first technological prototype of ILC: the **SDHCAL**

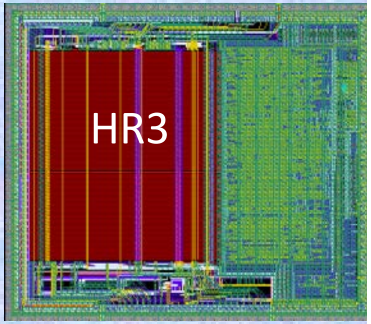



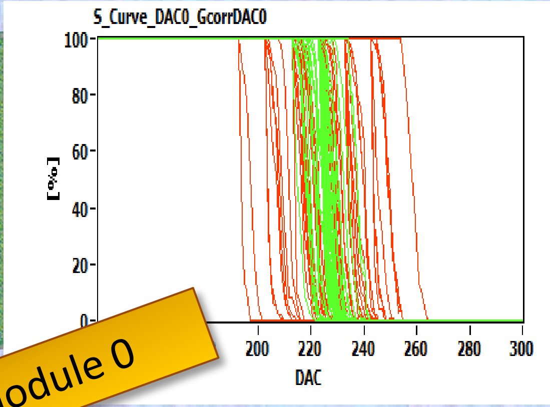




50 m^2 GRPC detector conceived and built, 10500 ASIC tested, 50 large electronic boards assembled and 50 cassettes completed

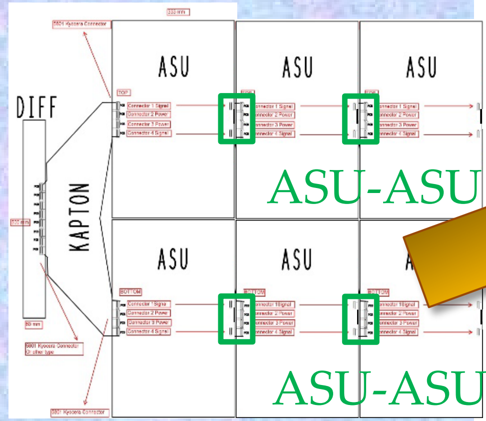
Towards the ILD SDHCAL Module 0: LP with 3rd generation of readout electronics

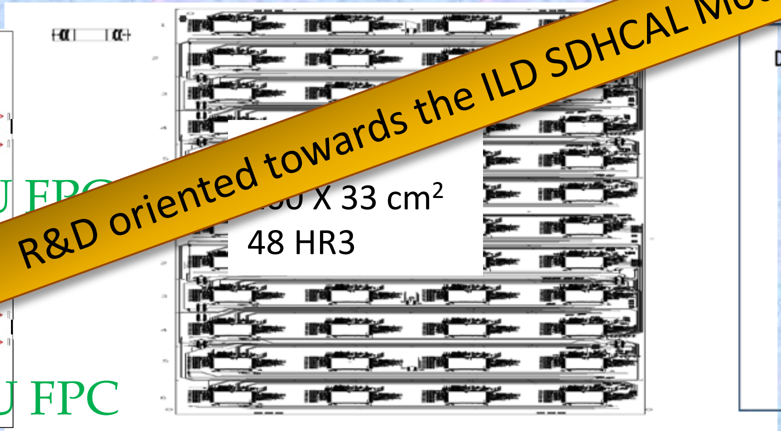
- 7500 HR3 (zero-suppres., I2C,…) are produced and tested.
- New ASUs to cover large detectors (> 2m^2) are designed and to be produced shortly
- New acquisition boards are designed and
- New schemes for large detectors are being tested
- New mechanical welding process (EBW) are tested

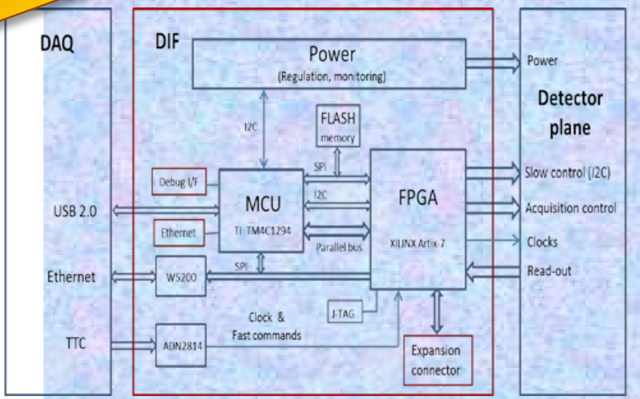


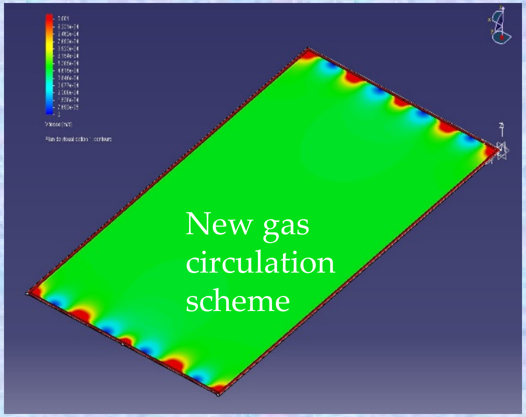


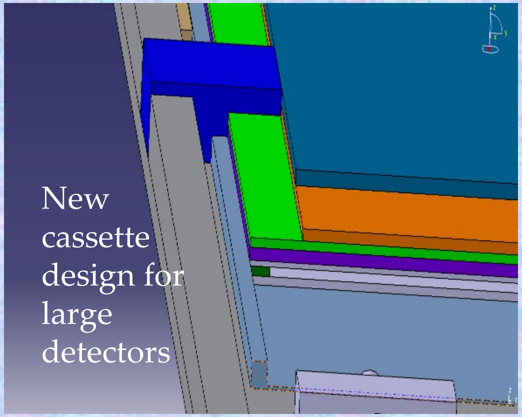
R&D oriented towards the ILD SDHCAL Module 0











I. Laktineh

LAPP: Micromegas R&D for SDHCAL

M. Chefdeville

SiD (semi-) digital HCAL at LAPP:

- Power-pulsing, embedded FE electronics + thin and large chambers

2007 : R&D starts at LAPP, guidance from Irfu

- Small MM prototypes with external analog electronics (Gassiplex)

2008-2011: LC-like prototypes – 32x48 cm2 Bulk MM and MICROROC ASICs

- 1x1 m2 prototypes of 6 units in 1 gas chamber

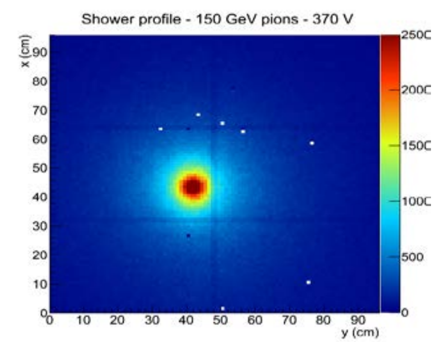
2011-2013: Resistive prototypes : different geometries on small prototypes with external electronics

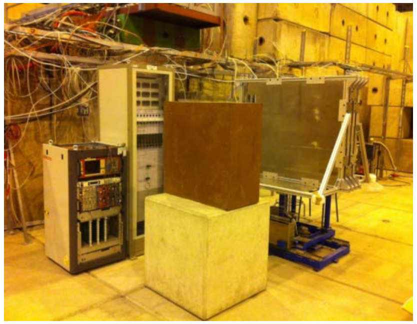
2014-2015 : Optimisation of one resistive geometry for high-rate (small prototypes)

- 2016 - : LC-like spark-less prototypes
  - From 10x10 cm2 resistive prototypes to 50x50 cm2 resistive
  - Possibly a small calorimeter prototypes with RD51-collalaborators

2008-2011: Large-area prototypes of 1x1 m² with embedded front-end electronics

- ➢ Micromegas with 1 x 1 cm2 pads
  → ~37,000 readout channels
- ➢ Interspersed in RPC-SDHCAL
  (use SDHCAL to reconstruct shower start!)

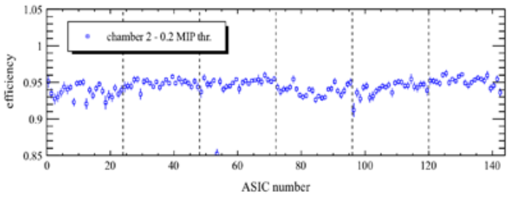




Measurements with MIPs

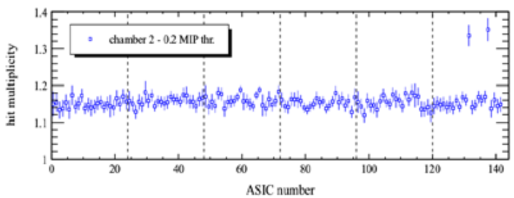
High efficiency > 95 %, hit multiplicity close to 1

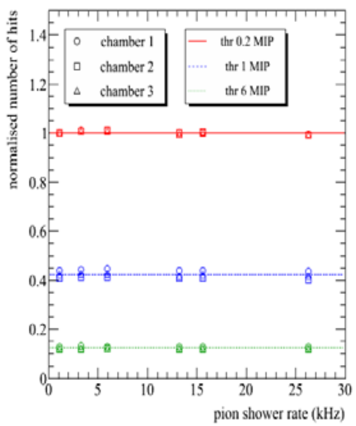
Very good uniformity



Measurement in pion showers

No effect of (pion shower) particle rate on response



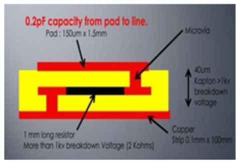


LAPP: Micromegas R&D for SDHCAL

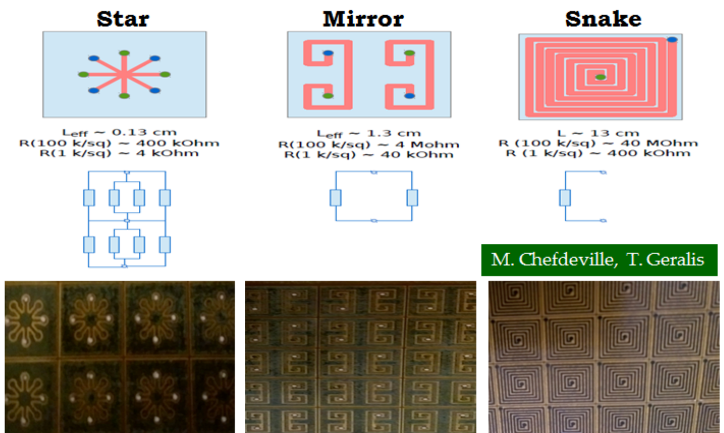
M. Chefdeville

Optimisation:
→ reduce resistivity and evacuation time but still suppress sparking

– "Vertical" evacuation of charge using buried resistors, proposed by Rui de Oliveira



– Ongoing program: Vary the RC, measure the linearity (rate & dE/dx scans), check sparking

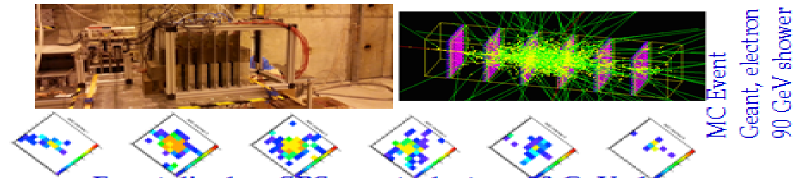


Real R1 values: 400 -750 KOhms with 100KΩ/Sq

Real R1 values: 4 MOhms with 100KΩ/Sq

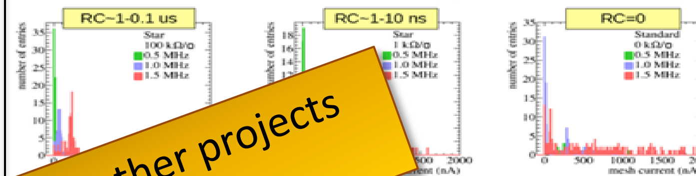
Real R1 values: 40 MOhms With 100KΩ/Sq

July 2015: Testbeam at SPS: μ, π and e beams



Event display: SPS event, electron 90 GeV shower

Monitor currents at electron shower maximum



RC: behaves like Non-resistive

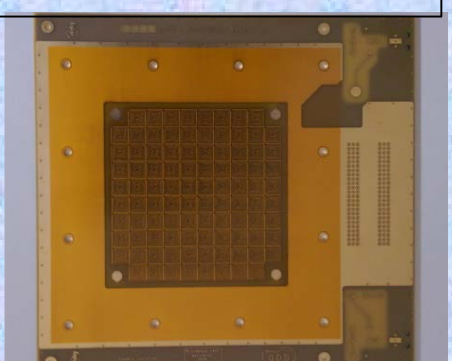
Non-resistive

R&D oriented towards ILC with synergies to other projects (collaboration LAPP - Irfu - Demokritos)

Use at future LC or the HL-LHC:

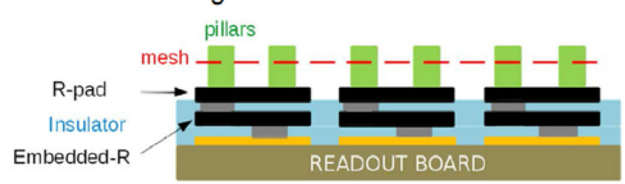
- Operation at high rates
- Suppress discharges … linearity
- High granularity … calorimetry,
- Small pads ~1x1 cm²,
- Large dynamic range (1 – 100s of MIPs)

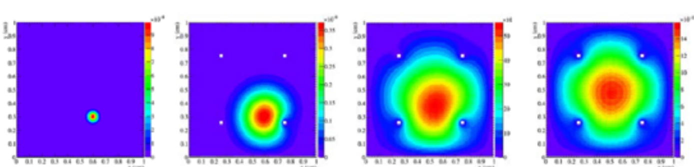
PCB with pads & resistive pattern

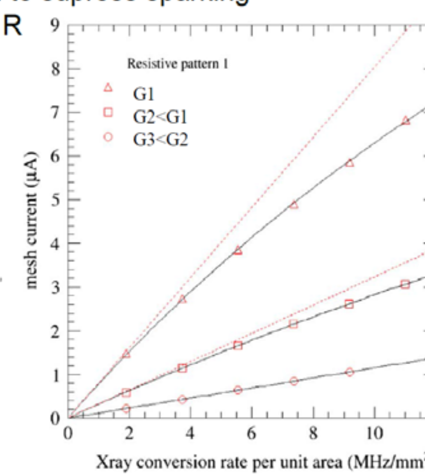


… resistive electrodes
… charge-up of anode when avalanche diverges → quenching
How low can we reduce the resistance without sparking ?

Small 10x10 cm² prototypes with « burried resistor » configuration (LAPP-Irfu-Demokritos)
Withstand huge flux : proportional region extends up to MHz/mm²
Also : very small resistance values are needed to supress sparking
Modelling studies to understand this threshold R





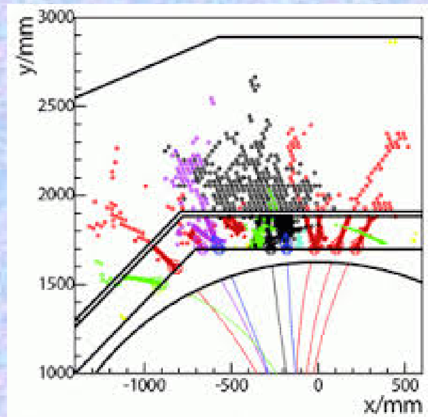


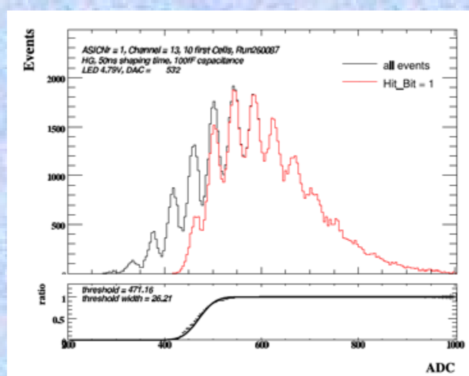
French Contribution: OMEGA Chips for CALICE

R&D on imaging calorimetry:

→ Particle Flow Algorithms

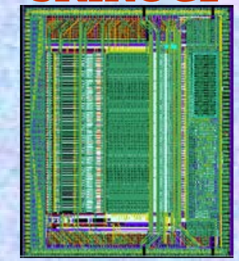
- Electronics crucial (low noise, low power, fully integrated)
- Several innovative features (power pulsing, SiPM…)
- Validation of technological prototypes
- Worldwide collaboration
- 4 chips produced : SKIROC, SPIROC, HARDROC, MICROROC



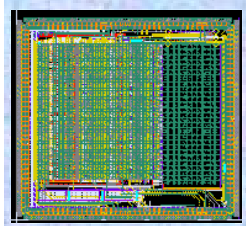


Ch. De La Taille

SKIROC2

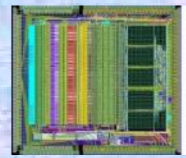


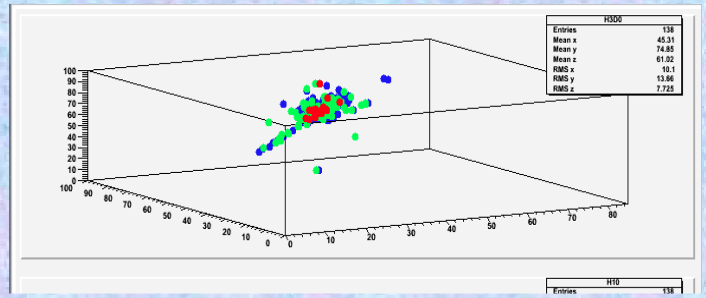
SPIROC2



HARDROC2

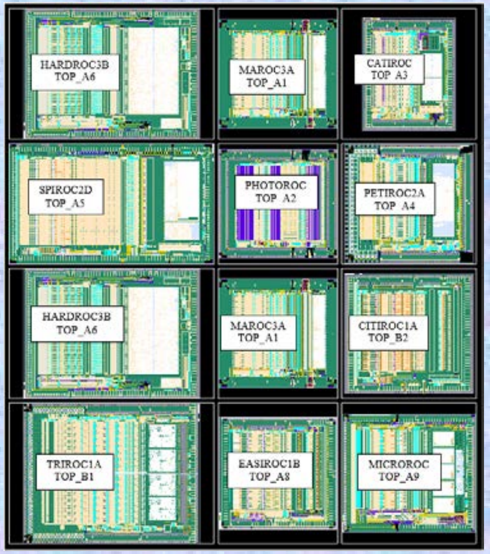
MICROROC



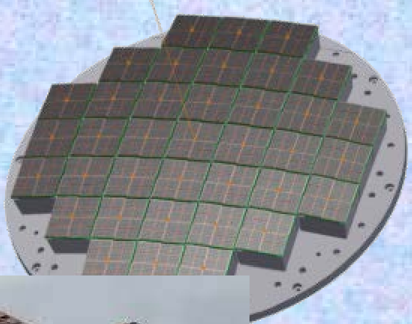


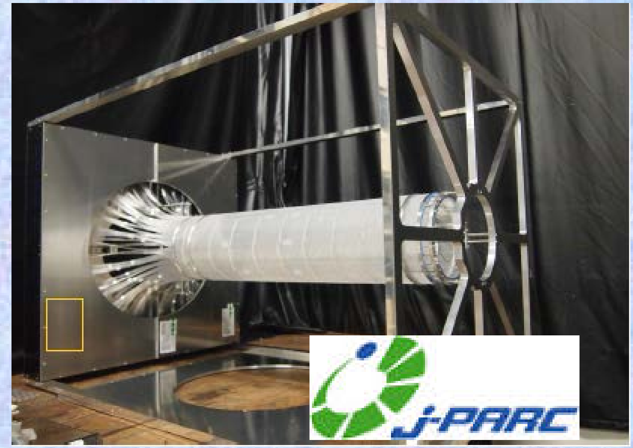
OMEGA Chips for Imaging Calorimetry

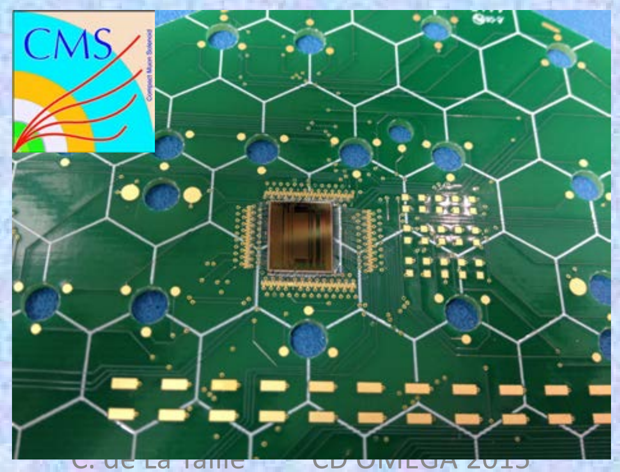
- 3 production runs in 2010, 2015 and 2016
  - Several hundreds of chips available
  - Equiped all CALICE prototypes (except US DHCAL)
- Re-used by many experiments outside ILC:
  - EASIROC for muon tomography and nuclear physics (E740 JPARC)
  - CITIROC for CTA small telescopes
  - SKIROC2 for CMS HGCAL



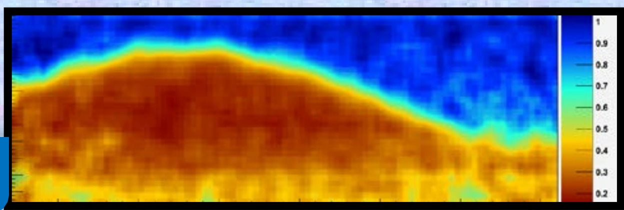
Ch. De La Taille



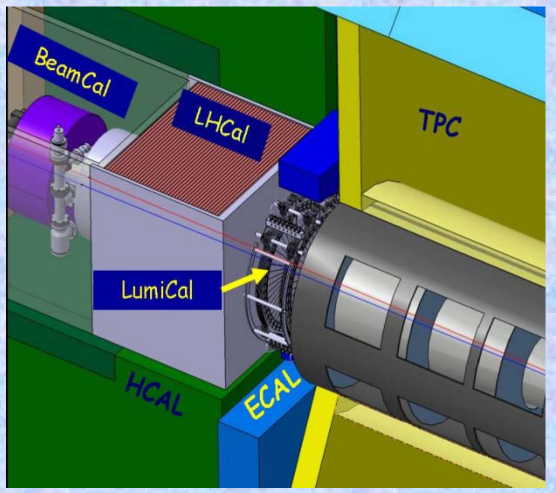


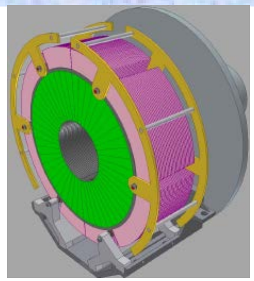


MU-RAY

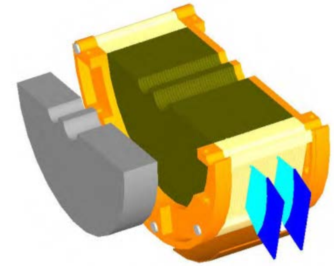


Forward Calorimetry R&D: FCAL Collaboration





LumiCal:
→ precise luminosity measurement
10^{-3} - 500 GeV @ ILC
10^{-2} - 3 TeV @ CLIC



BeamCal:
→ inst. lumi measurement / beam tuning, beam diagnostics

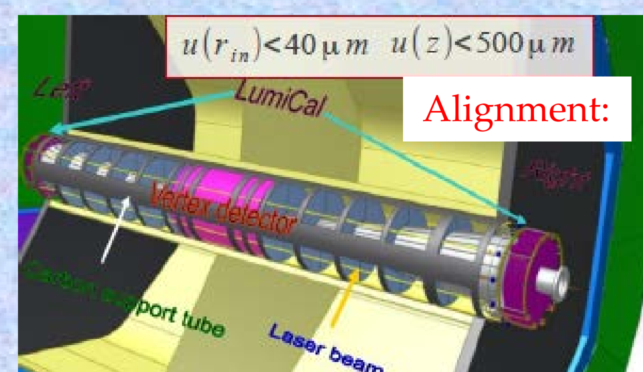
LumiCal: Two Si-W sandwich EM calo at a ~ 2.5 m from the IP (both sides)
30 / 40 (ILC/CLIC) tungsten disks of 3.5 mm thickness

BeamCal: very high radiation load (up to 1MGy/ year) → similar W-absorber, but radiation hard sensors (GaAs, CVD diamond)

BeamCal Sensors

LumiCal ASIC:

Alignment:



Laser alignment system (LAS) based on Frequency Scanning Interferometry (FSI)

- Unique contributions to the ILC DBD, the CLIC CDR, and to the detector concepts ILD and SiD

- Successful prototyping and test of major components in the beam → final preparation of a 'large testbeam paper' (2010 - 2012 results) → the performance of fully assembled sensor planes matches the requirements

French contribution (up to ~2010):

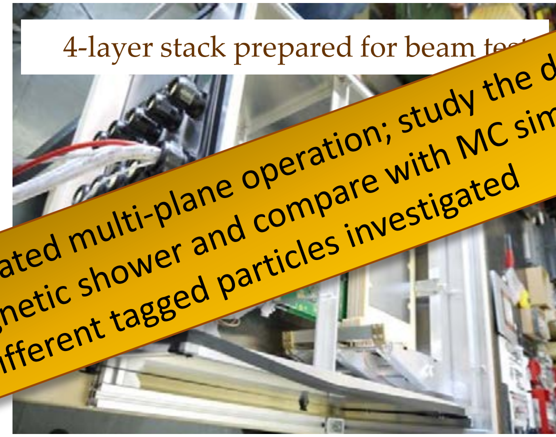
LAL (P. Bambade) → FCAL/MDI studies; feasibility to use diamond sensors; beam-beam interactions studies

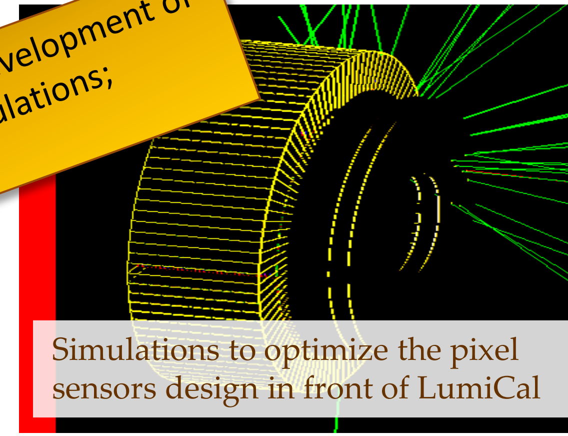
FCAL R&D: Ongoing Activities

W. Lohmann

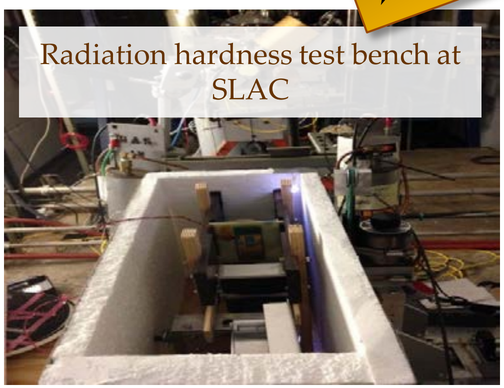
Test-beam (October 2014) at CERN:

- Four sensor layers assembled with ASICs in a 10 GeV mixed beam
- Acquire expertise to operate a multi-layer structure
- Data-MC comparison


4-layer stack prepared for beam te


Simulations to optimize the pixel sensors design in front of LumiCal

- 2014: Demonstrated multi-plane operation; study the development of the electromagnetic shower and compare with MC simulations;
- Response to different tagged particles investigated


Radiation hardness test bench at SLAC

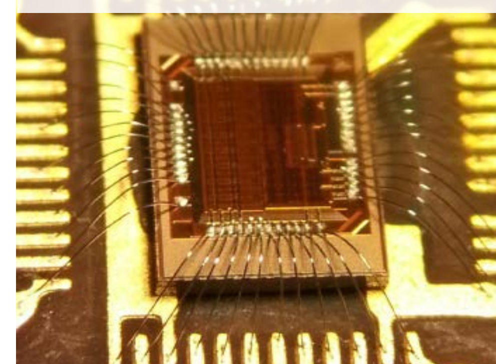
Sensor R&D:

- Pixel sensors in front of LumiCal (improve shower position reconstruction, alignment)
- Edgeless sensors for LumiCal (to reduce dead areas)
- Radiation hardness studies in a 'realistic' environment (T506 at SLAC) of the Si and GaAs sensors

ASIC development (130 nm CMOS):

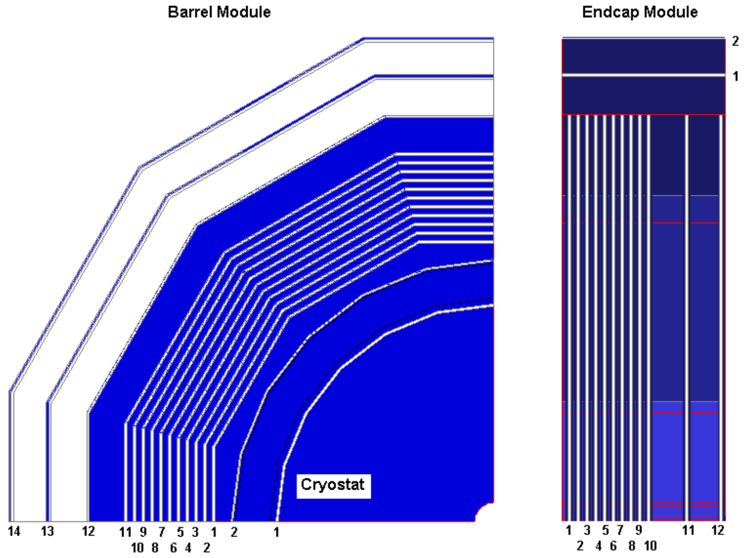
- 8 channel FE ASIC, dual gain, low power consumption; 8 channel SAR ADC
- Prototypes of both ASICs are tested and match the specification
- Power pulsing implemented
- Next step will be to enhance the number of channels per chip, integrate in a readout board

8 channel FE ASIC in the test bench



ILD Muon System / Tail Catcher System

V. Saveliev



Main Tasks:

- Efficient Identification of Muons
- Measurement of the Energy Leakage from Hadron Calorimeter (especially if HCAl inside the magnet)

Historical aspects:

❖ 2000: Muon System R&D started since TESLA proposal CALICE HCAL groups involved in Muon system R&D; some test-beams are common

❖ 2006: more active R&D, US groups joined; development of special facility (Fermilab) for the scintillator strip with embedded WLS production

Instrumentation of ILD Muon/Tail Catcher System

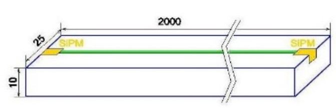
Main option – Scintillation strips with WLS and SiPM readout)

Barrel: 11stereo Layer, absorber 10 cm (Tail Catcher Function) + 3 stereo Layers, absorber 60 cm

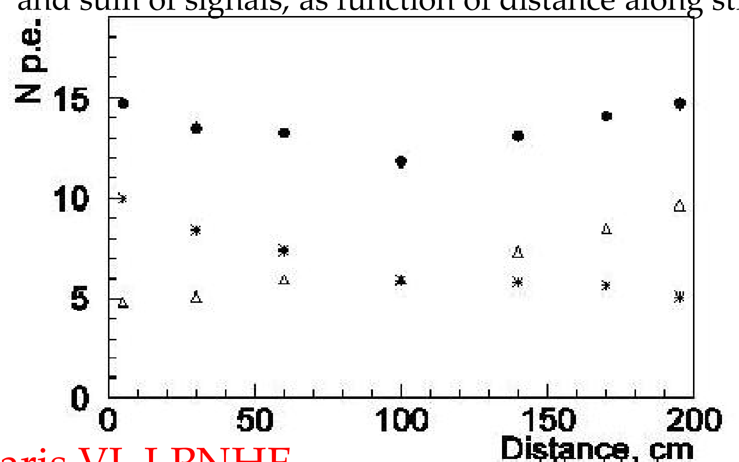
Endcap: 10 stereo Layers, absorber 10 cm,
+ 2 stereo Layers, absorber 60 cm

Detection Element :

Scintillation Strip with WLS and SiPMs on both side



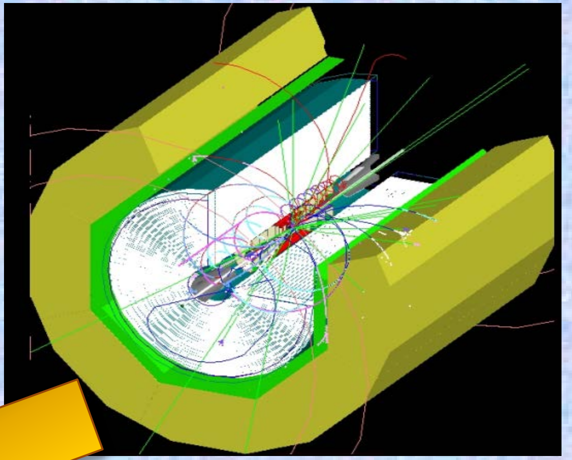
Number of photons detected from both side by SiPMs and sum of signals, as function of distance along strip



French groups (past activities): Paris VI, LPNHE

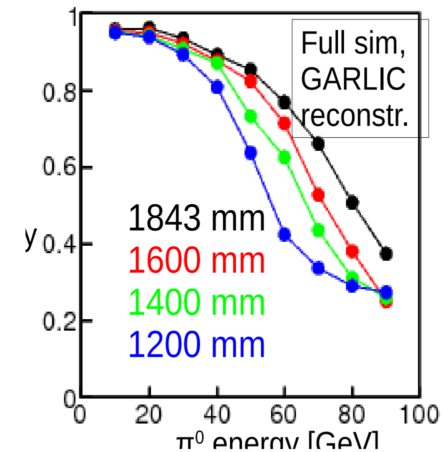
Linear Collider Software

French contributions to software packages:
simulation / reconstruction:



- Mokka (**IN2P3**): Framework for all ILD and CLIC-dp detector versions, since 1999 → To be superseded by DD4HEP

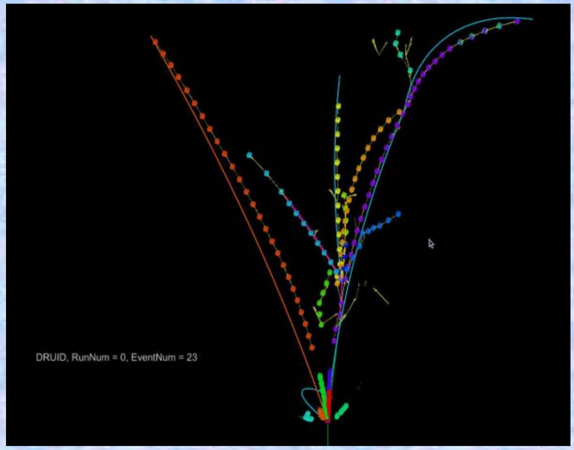
see talk of B. Li



Advanced Reconstruction Algorithms for Highly Granular Calorimeters:

- GARLIC (**LLR**, Tokyo): Dedicated reconstruction for photons

- Arbor (**LLR, Lyon**): Particle Flow reconstruction based on branching structure of particle showers

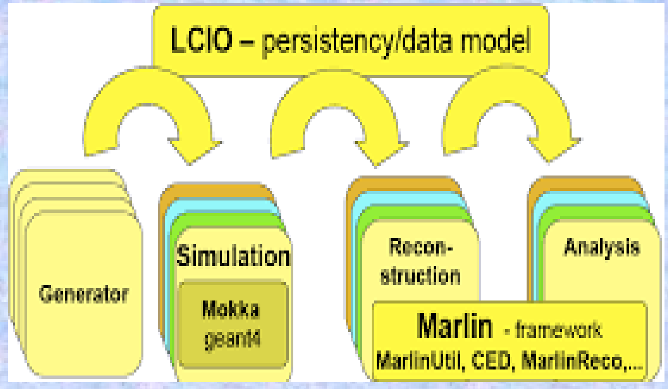


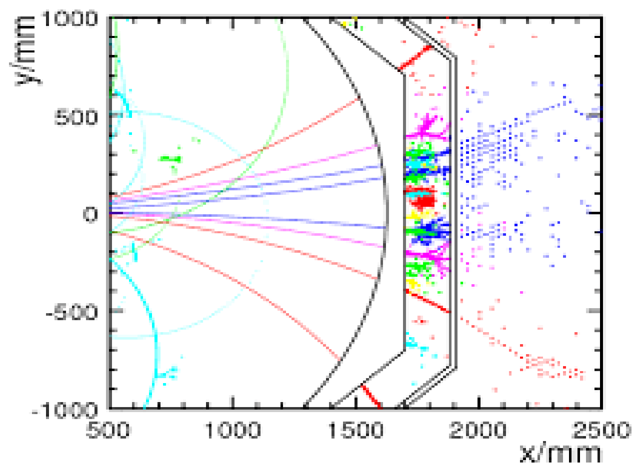
F. Gaede,
J. Strube

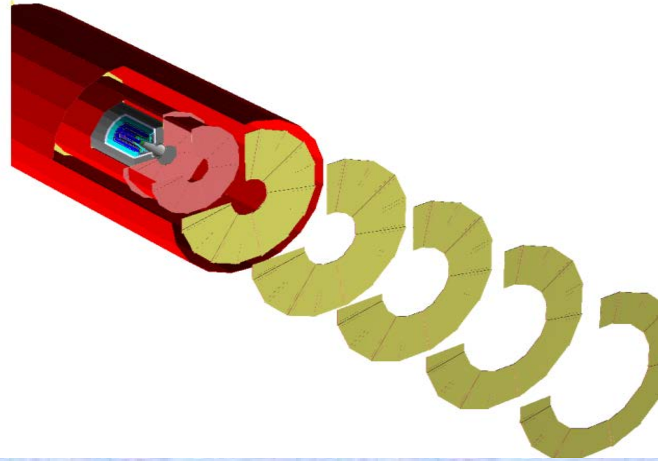
Common Linear Collider Software

- LCIO (DESY, SLAC, **IN2P3**): Common event data model, allows easy exchange of tools
- LCFIPlus (Tokyo) vertex reconstruction / flavor tagging
- PandoraPFA (Cambridge, CERN): PFA event reconstruction
- DD4HEP and friends (DESY, CERN): Comprehensive suite of simulation and reconstruction tools
  - Replaces Mokka (LLR)

F. Gaede,
J. Strube







Summary and Outlook

- Linear Collider R&D remains a very active field
  → synergies exists with other projects HL-LHC, STAR, ALICE, Belle2, …
  → important to keep an eye on new technologies, since the existing designs were started a long time ago

.

FRENCH COMMUNITY has played key roles in the ILC R&D (since TESLA)

Today's, French groups are still very active
→ R&D and engineering efforts are largely constrained by the available resources